74HC2G16; 74HCT2G16

Dual buffer gate

Rev. 3 — 5 December 2023 Product data sheet

1. General description

The 74HC2G16; 74HCT2G16 is a high-speed Si-gate CMOS device.

The 74HC2G16; 74HCT2G16 provides two buffers.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- Unlimited input rise and fall times
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G16GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74HCT2G16GW				
74HC2G16GV	-40 °C to +125 °C	SC-74; TSOP6	plastic surface-mounted package; 6 leads	SOT457
74HCT2G16GV				

4. Marking

Table 2. Marking

Type number	Marking code[1]
74HC2G16GW	P6
74HCT2G16GW	U6
74HC2G16GV	P6
74HCT2G16GV	U6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

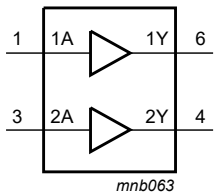


Fig. 1. Logic symbol

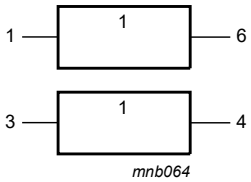


Fig. 2. IEC logic symbol

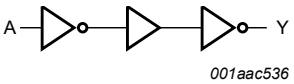


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

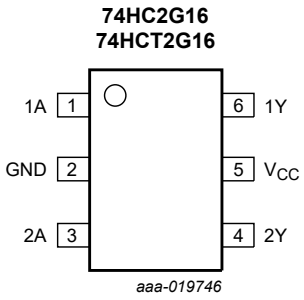


Fig. 4. Pin configuration SOT363-2 (TSSOP6) and SOT457 (SC-74; TSOP6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A	1	data input
GND	2	ground (0 V)
2A	3	data input
2Y	4	data output
V_{CC}	5	supply voltage
1Y	6	data output

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	**nY**
L	L
H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	[1]	-	±25	mA
I_{CC}	supply current		[1]	-	+50	mA
I_{GND}	ground current		[1]	-	-50	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.
For SOT457 (SC-74; TSOP6) package: P_{tot} derates linearly with 4.1 mW/K above 89 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC2G16						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
t_r	rise time	except for Schmitt trigger inputs				
		V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	-	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
t_f	fall time	except for Schmitt trigger inputs				
		V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	-	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
74HCT2G16						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
t_r	rise time	except for Schmitt trigger inputs				
		V_{CC} = 4.5 V	-	-	500	ns
t_f	fall time	except for Schmitt trigger inputs				
		V_{CC} = 4.5 V	-	-	500	ns

10. Static characteristics

Table 7. Static characteristics for 74HC2G16

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	4.18	4.32	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.68	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 6.0 V	-	-	1.0	µA
C_I	input capacitance		-	1.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	4.13	-	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.63	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 6.0 V	-	-	10.0	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 6.0 V	-	-	20.0	µA

Table 8. Static characteristics for 74HCT2G16

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	4.18	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	300	µA
C_I	input capacitance		-	1.5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	4.13	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V	-	-	10.0	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	375	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
I_I	input leakage current	V_I = GND or V_{CC}; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	410	µA

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

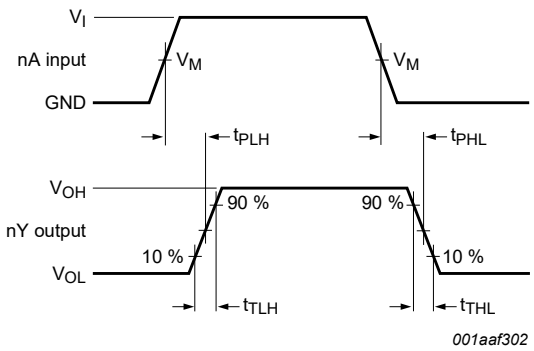
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G16										
t_{pd}	propagation delay	nA to nY; see Fig. 5 [1]								
		V_{CC} = 2.0 V; C_L = 50 pF	-	29	75	-	95	-	125	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	9	15	-	19	-	25	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	8	13	-	16	-	20	ns
t_t	transition time	nY; see Fig. 5 [2]								
		V_{CC} = 2.0 V; C_L = 50 pF	-	18	75	-	95	-	125	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	6	15	-	19	-	25	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	5	13	-	16	-	20	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [3]	-	10	-	-	-	-	-	pF
74HCT2G16										
t_{pd}	propagation delay	nA to nY; see Fig. 5 [1]								
		V_{CC} = 4.5 V; C_L = 50 pF	-	10	18	-	23	-	29	ns
t_t	transition time	nY; see Fig. 5 [2]								
		V_{CC} = 4.5 V; C_L = 50 pF	-	6	15	-	19	-	25	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V [3]	-	9	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}

[2] t_t is the same as t_{TLH} and t_{THL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



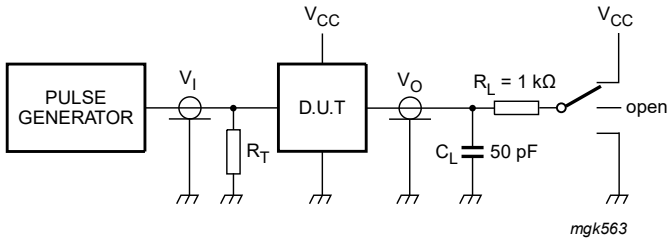
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig. 5. The data input (nA) to output (nY) propagation delays and output transition times

Table 10. Measurement points

Type	Input			Output
	V_M	V_I	$t_r = t_f$	V_M
74HC2G16	$0.5V_{CC}$	GND to V_{CC}	6.0 ns	$0.5V_{CC}$
74HCT2G16	1.3 V	GND to 3.0 V	6.0 ns	1.3 V



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

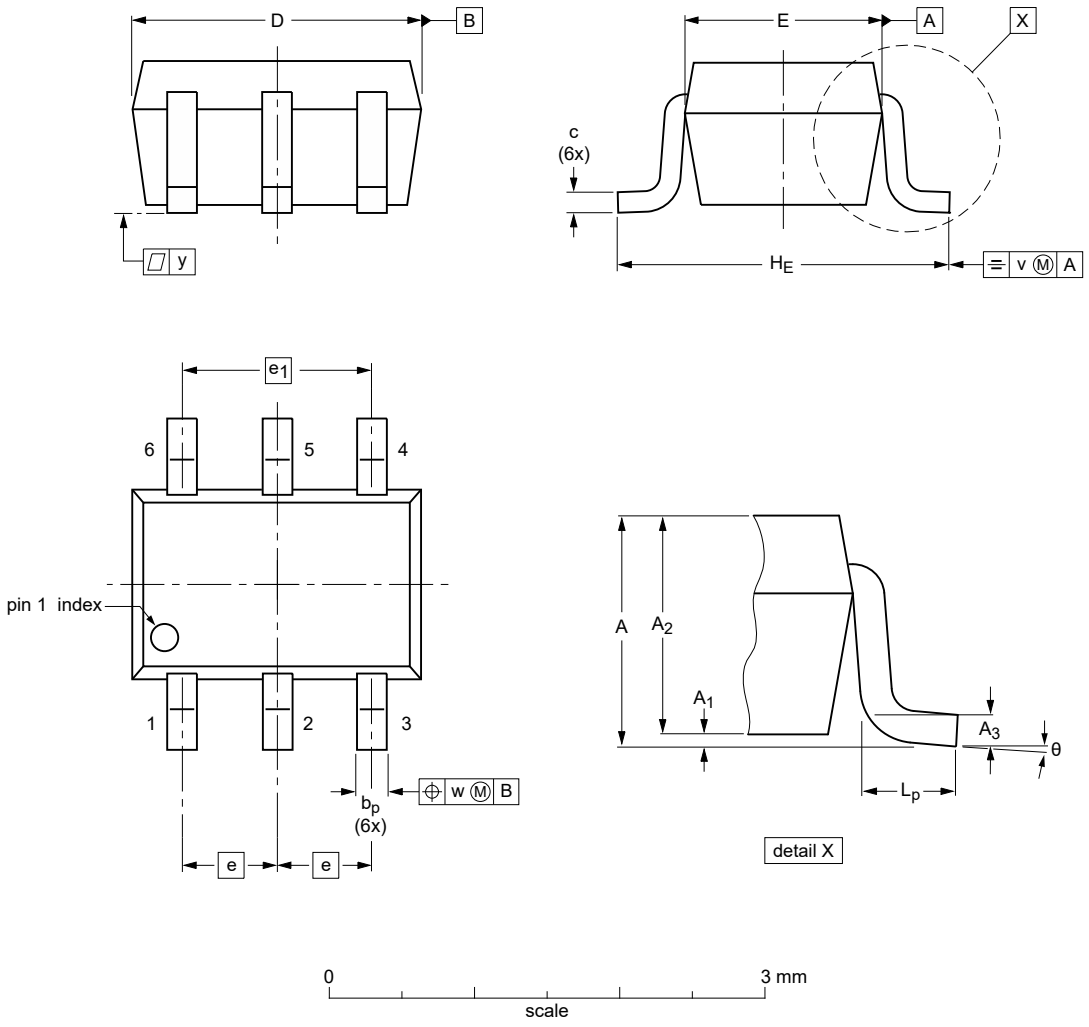
Fig. 6. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Test
	V_I	t_r, t_f	t_{PHL}, t_{PLH}
74HC2G16	GND to V_{CC}	6 ns	open
74HCT2G16	GND to 3.0 V	6 ns	open

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

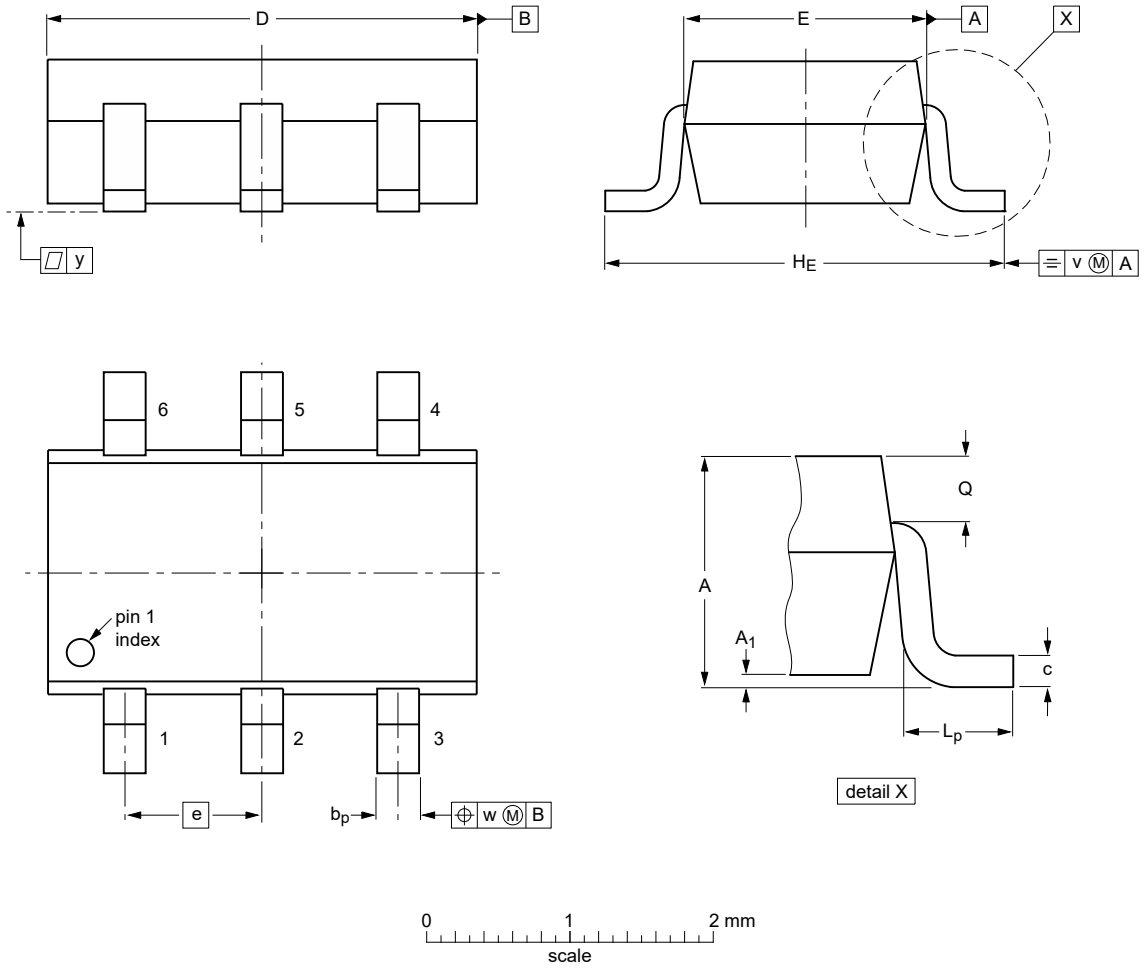
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT363-2		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 7. Package outline SOT363-2 (TSSOP6)

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads **SOT457**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	max	1.1	0.1	0.40	0.26	3.1	1.7		3.0	0.6	0.33	0.2	0.2	0.1
	nom							0.95						
	min	0.9	0.013	0.25	0.10	2.7	1.3		2.5	0.2	0.23			

sot457_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~06-03-16~~ 18-11-27

Fig. 8. Package outline SOT457 (SC-74; TSOP6)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G16 v.3	20231205	Product data sheet	-	74HC_HCT2G16 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT2G16 v.2	20220202	Product data sheet	-	74HC_HCT2G16 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). • Section 8: Derating values for P_{tot} total power dissipation updated. • Fig. 8: Package outline drawing SOT457 (SC-74; TSOP6) updated.			
74HC_HCT2G16 v.1	20151102	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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