

## Am29833A/Am29853A

## **Parity Bus Transceivers**

#### DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceivers for processor organized devices
  - T-R delay = 6 ns typical
  - Ri-Parity delay = 9 ns typical
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- 200 mV minimum input hysteresis (Commercial) on input data ports
- High drive capability:
  - 48 mA Commercial lou
- Higher speed, lower power versions of the Am29833 & Am29853

#### GENERAL DESCRIPTION

The Am29833A and Am29853A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an ERR flag showing the result of the parity test.

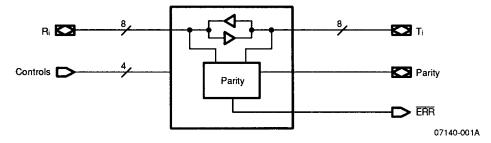
In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector  $\overline{ERR}$  output. The  $\overline{CLR}$  input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the  $\overline{EN}$  and  $\overline{CLR}$  controls are used to pass, store, sample or clear the error flag output. When both output enables

are disabled in the Am29853A and Am29833A, the parity logic defaults to the transmit mode, so that the ERR pin reflects the parity of the R port.

The output enables,  $\overline{OER}$  and  $\overline{OET}$ , are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both  $\overline{OER}$  and  $\overline{OET}$  simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

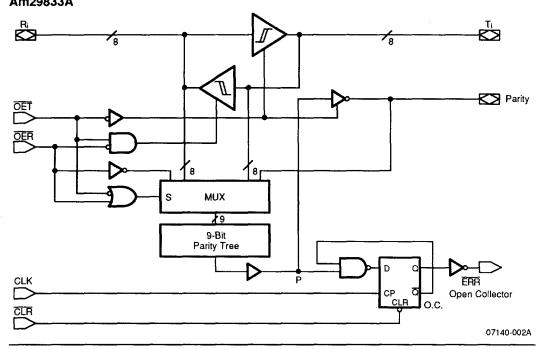
Each of these devices is produced with AMD's proprietary IMOX<sup>TM</sup> bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability.

#### SIMPLIFIED BLOCK DIAGRAM

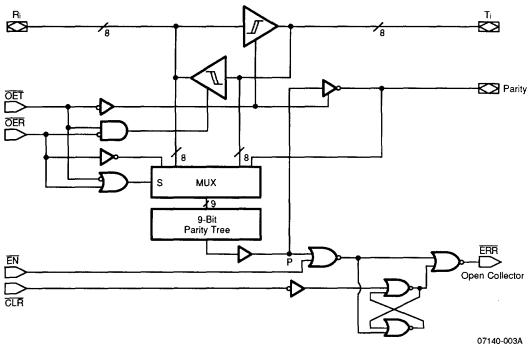


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## BLOCK DIAGRAMS Am29833A



## Am29853A

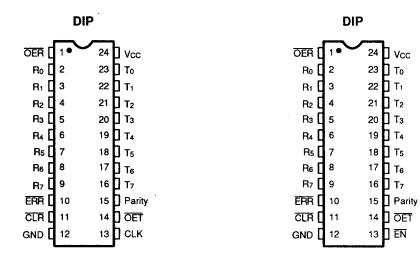




## CONNECTION DIAGRAMS (Top View)

#### Am29833A

#### Am29853A



07140-004A

07140-005A

## FUNCTION TABLE Am29833A (Register Option)

	Inputs						Out	puts				
ŌĒŤ	ŌĒR	CLR	CLK	Ri	Sum of H's of Ri	Ti	Sum of H's (Ti+ Parity)	Ri	Ti	Parity	ERR	Function
L L L	H H H	X X X	X X X	III	ODD EVEN ODD EVEN	NA NA NA NA	NA NA NA NA	NA NA NA NA	H L L	LHLH	NA NA NA NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
H H H	L	I	<b>†</b> † † †	NA NA NA NA	NA NA NA NA	H H L	ODD EVEN ODD EVEN	HLL	NA NA NA	NA NA NA NA	IJIJ	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
Х	Х	L	Х	Х	Х	Х	Х	Х	Х	Х	Н	Clear error flag register.
H	H	ΙJ	X X	X X	×	X	X X	Z Z	Z Z	Z Z	• т	Both transmitting and receiving paths are disabled.
HULLL	H H L L L L	HHXXXX	↑	- エエエー-	ODD EVEN ODD EVEN ODD EVEN	X X NA NA NA NA	X X NA NA NA	Z Z NA NA NA NA	2 Z H H L L	Z Z H L H L	T - A A A A	Parity logic defaults to transmit mode. Forced-error checking.

H = HIGH

L = LOW

↑ = LOW-to-HIGH Transition

X = Don't Care

Z = High Impedance

NA= Not Applicable

\* = Store the State of the Last Receive Cycle ODD = Odd Number

EVEN= Even Number

i = 0, 1, 2, 3, 4, 5, 6, 7



## FUNCTION TABLE Am29853A (Latch Option)

Inputs									Out	puts		
ŌĒĪ	ŌER	CLR	ĒŃ	Ri	Sum of H's of Ri	Ti	Sum of H's (T <sub>i+</sub> Parity)	Ri	T <sub>i</sub>	Parity	ERR	Function
L	H H H	X X X	× × ×	HHLL	ODD EVEN ODD EVEN	NA NA NA	NA NA NA NA	NA NA NA	H L L	L H L H	NA NA NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
<b>111</b>	-1 -1 -1	نب ئاس ئاس ئاس		NA NA NA	NA NA NA NA	IIJJ	ODD EVEN ODD EVEN	HHLL	NA NA NA	NA NA NA	TJTJ	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
<b>T T T</b>	L L L	IIII		NA NA NA	NA NA NA NA	I I	ODD EVEN ODD EVEN	HLLL	NA NA NA	NA NA NA	HLHL	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
Н	L	Н	Н	NA	NA	Х	Х	Х	NA	NA	٠	Store the state of error flag latch.
Х	X	L	Н	Х	Х	Х	×	X	NA	NA	Н	Clear error flag latch.
H H H H	IIII	ΗLXX	HHLL	X X L H	X X ODD EVEN	X X X	× × ×	Z Z Z Z	Z Z Z Z	Z Z Z Z	• ##-	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
L L L	L L L	X X X	X X X	H H L	ODD EVEN ODD EVEN	NA NA NA	NA NA NA NA	NA NA NA NA	H H L L	H L H	NA NA NA NA	Forced-error checking.

H = HIGH

Z= High Impedance

ODD = Odd Number

L = LOW

X = Don't Care

NA= Not Applicable

EVEN= Even Number

↑ = LOW-to-HIGH Transition

\*= Store the State of the Last

Receive Cycle

i = 0, 1, 2, 3, 4, 5, 6, 7

# TRUTH TABLES Error Flag Output

### Am29833A

In	Inputs		Outputs Pre-state	Output	
CLR	CLK	Point "P"	ERR <sub>n-1</sub>	ERR	Function
Н	<b>↑</b>	Н	Н	Н	
Н	<b>↑</b>	×	L	L	Sample (1's Capture)
Н	1	L	X	L	
L	Х	X	X	Н	Clear

Note:

OET is HIGH and OER is LOW.

#### Am29853A

Inputs		Internal to Device	Outputs Pre-state	Output			
EN	EN CLR		ERR <sub>n-1</sub>	ERR	Function		
L	L	L	Х	L	Door		
L	L	H	×	Н	Pass		
L	Н	L	X	L			
L	Н	×	L	L	Sample (1's Capture)		
L	н	н	н	Н			
Н	L	Х	Х	Н	Clear		
Н	Н	×	L	L	Store		
_н	Н	x	н	н	Store		

Note:

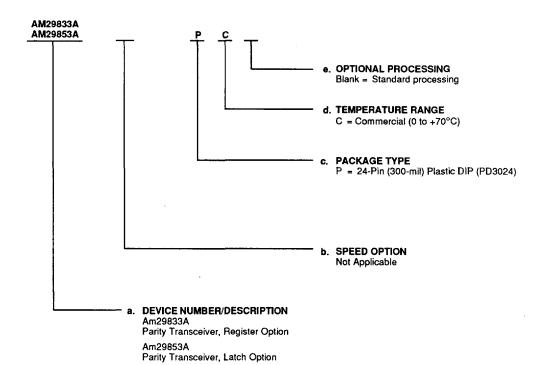
OET is HIGH and OER is LOW.



## ORDERING INFORMATION Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations							
AM29833A	PC						
AM29853A	]PC						

#### **Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

#### PIN DESCRIPTION Am29833A/Am29853A

#### **OFR**

#### Output Enable Receive (Input, Active LOW)

When LOW in conjunction with OET HIGH, the devices are in the Receive mode (R<sub>i</sub> are outputs, T<sub>i</sub> and Parity are inputs).

#### **OET**

#### Output Enable Transmit (Input, Active LOW)

When LOW in conjunction with OER HIGH, the devices are in the Transmit mode (Ri are inputs, Ti and Parity are outputs).

#### R

#### Receive Port (Input/Output, Three-State)

 $R_{\rm i}$  are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

#### $T_{i}$

#### Transmit Port (Input/Output, Three-State)

T<sub>i</sub> are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

#### Parity

#### Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the Ti and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

#### Am29833A Only

#### ERR

#### Error Flag (Output, Open Collector)

In the Receive mode, the parity of the T<sub>i</sub> bits is calculated and compared to the Parity input. ERR goes LOW when the comparison indicates a parity error. ERR stays LOW until the register is cleared.

#### **CLR**

#### Clear (Input, Active LOW)

When CLR goes LOW, the Error Flag Register is cleared (ERR goes HIGH).

#### CLK

#### Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

#### Am29853A Only

#### **ERR**

#### Error Flag (Output, Open Collector)

In the Receive mode, the parity of the Tibits is calculated and compared to the Parity input. ERR goes LOW when the comparison indicates a parity error. ERR stays LOW until the latch is cleared.

#### CLR

#### Clear (Input, Active LOW)

When  $\overline{\text{CLR}}$  goes LOW, and  $\overline{\text{EN}}$  is HIGH, the Error Flag latch is cleared ( $\overline{\text{ERR}}$  goes HIGH).

#### ĒΝ

#### Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.



## **ABSOLUTE MAXIMUM RATINGS**

Storage Temperature . -65°C to +150°C

Ambient Temperature with

Power Applied -55 to +125°C

Supply Voltage to Ground

Potential Continuous -0.5 V to +7.0 V

DC Voltage Applied to Outputs For

High Output State -0.5 V to +5.5 V

DC Input Voltage -1.5 V to +6.0 V

DC Output Current, Into Outputs 100 mA
DC Input Current -30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

#### **OPERATING RANGES**

Commercial (C) Devices

Ambient Temperature (T<sub>A</sub>) 0 to +70°C Supply Voltage (Vcc) +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

#### DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Condition	Min.	Max.	Unit		
Vон	Output HIGH Voltage	Vcc = 4.5 V,		I <sub>OH</sub> = -15 mA	2.4		
	Except (ERR)	VIN = VIHOT VIL		Iон = -24 mA	2.0		V
Vol	Output LOW Voltage	Vcc = 4.5 V, ERR Ic		loL = 48 mA		0.5	٧
		VIN= VIHOR VIL	All Other Outputs	I <sub>OL</sub> = 48 mA		0.5	V
ViH	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)				V
VIL	Input LOW Voltage	Guaranteed Inp all inputs (Note		8.0	٧		
Vı	Input Clamp Voltage	Vcc = 4.5 V, IIN		-1.2	V		
VHYST	Hysteresis for Inputs Ri, Ti		200		m۷		
İZL	I/O Port LOW Current	Vcc = 5.5 V, VIN		-550	μΑ		
l și_	Input LOW Current	Vcc = 5.5 V, Vin = 0.4 V				-0.5	mA
lıн	Input HIGH Current	Vcc = 5.5 V, Vin = 2.7 V				50	μΑ
li .	Input HIGH Current	Vcc = 5.5 V, Vin	Vcc = 5.5 V, Vin = 5.5 V				μΑ
İZH	I/O Port HIGH Current	Vcc = 5.5 V, Vin	ı = 2.7 V			100	μΑ
lzı	I/O Port HIGH Current	Vcc = 5.5 V, VI	ı = 5.5 V			150	μΑ
Isc	Output Short-Circuit Current	Vcc = 5.5 V, Vo	-75	-250	mA		
loff	Bus Leakage Current	Vcc = 0 V, Vo =		100	μΑ		
lcc	Power Supply Current	Vcc = 5.5 V		Outputs LOW		180	
		Outputs Loaded	t	Outputs HIGH		155	mA
				Outputs Hi-Z		170	

#### Notes:

- 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
- 2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.



## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions*	Min.	Max.	Unit
tры	Propagation Delay to Ri to Ti,				10	ns
tphL	Ti to Ri				10	ns
t <sub>PLH</sub>	Drama nation Dalou D. to David				15	ns
t <sub>PHL</sub>	Propagation Delay Ri to Parit	у			15	ns
tzн	Output Enable Time OER, OF	T to Ri, Ti		12		ns
tzı	and Parity				12	ns
tHZ	Output Disable Time OER, O	ET to Ri, Ti		12		ns
tız	and Parity		C <sub>L</sub> = 50 pF R <sub>1</sub> = 500 Ω		12	ns
ts	Ti, Parity to CLK Setup Time	(Note 1)		12		ns
tн	Ti, Parity to CLK Hold Time (I	Note 1)		0		ns
TREC	Clear (CLR _ ) to CLK Setu (Note 2)	p Time	$R_2 = 500 \Omega$	15		ns
. tpwH	Ota al Dala a Manue (Mana A)	HIGH		7		ns
tpwL	Clock Pulse Width (Note 1)	LOW		7		ns
tpwl.	Clear Pulse Width	LOW		7		ns
t <sub>PHL</sub>	Propagation Delay CLK to EF	R (Note 1)			12	ns
<b>t</b> PLH	Propagation Delay CLR to EF	₹ <b>R</b>			16	ns
tplH	Propagation Delay Ti, Parity t	o ERR			22	ns
tphL	(PASS Mode Only) Am29853	Α			18	ns
t <sub>PLH</sub>	December Dalay OFD to D	- ula			15	ns
<b>t</b> PHL	Propagation Delay OER to Pa	arity			15	ns

<sup>\*</sup>See test circuit and waveforms (Chapter 2).

#### Notes:

<sup>1.</sup> For Am29853A, replace CLK with EN.

<sup>2.</sup> Not applicable to Am29853A.