1.1 Scope.

This specification covers the requirements for a CMOS monolithic program sequencer.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-1401SD/883B
−2	ADSP-1401TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

ADSP-1401 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0			V_{DD} = max	V min
Clock Input High Voltage	V_{IHC}	−1, 2	3.0	3.0	3.0			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −1mA	V min
Digital Output Low Voltage	V_{OL}	−1, 2	0.6	0.6	0.6			V_{DD} = min I_{OL} = +3mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IN} = 0V	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IN} = max	μA max
Supply Current*	I_{DD1}	−1, 2	90	115	115			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	35	65	65			All V_{IN} = 2.4V	mA max
Clock HI*	t_{HI}	−1	50			60	60	Note 2	ns min
		−2	40			50	50	Note 2	ns min
Clock LO*	t_{LO}	−1	40			50	50	Note 2	ns min
		−2	30			40	40	Note 2	ns min
Instruction Setup Time*	t_{IS}	−1	36			45	45	Note 2	ns min
		−2	30			40	40	Note 2	ns min
Data Setup Time*	t_{DS}	−1, 2	10			15	15	Note 2	ns min
Input Signal Hold Time	t_{IH}	−1, 2	3			3	3	Note 2	ns min
Address Delay*[3]	t_{AD}	−1	35			45	45	Note 2, C = 50pF	ns max
		−2	25			35	35	Note 2, C = 50pF	ns max
Address Hold Time*	t_{AH}	−1, 2	3			1	1	Note 2	ns min
Output Data Delay*	t_{ODD}	−1	50			60	60	Note 2, C = 30pF	ns max
		−2	35			45	45	Note 2, C = 30pF	ns max
Output Data Disable Time*	t_{ODIS}	−1	20			25	25	Note 2	ns max
		−2	15			20	20	Note 2	ns max
Input Flag Setup Time (IR0 Masked)	t_{IFSM}	−1	15			20	20	Note 2, IR0 Masked	ns min
		−2	10			15	15	Note 2, IR0 Masked	ns min
Input Flag Setup Time* (No Constraints)	t_{IFSU}	−1	30			35	35	Note 2	ns min
		−2	26			30	30		

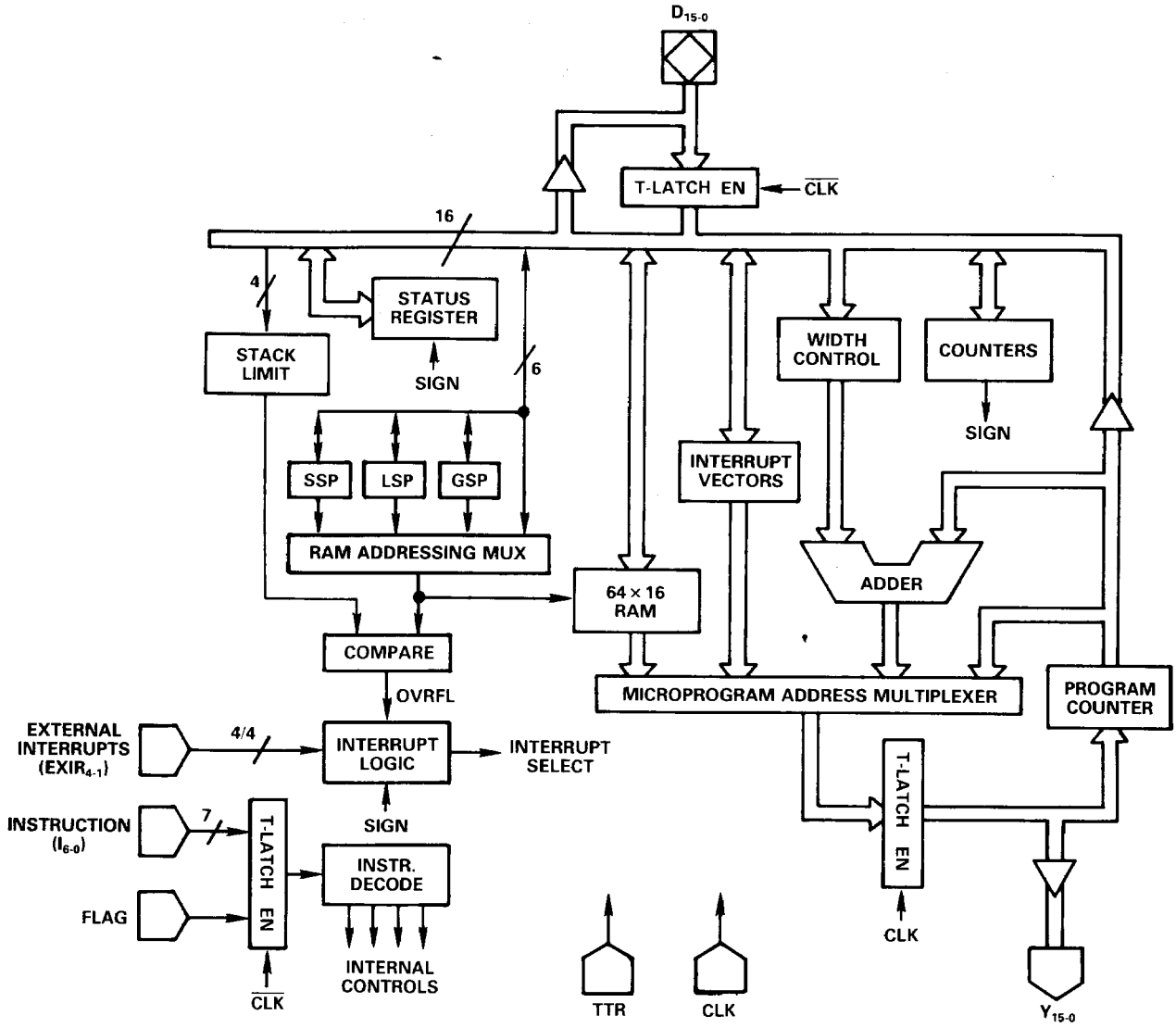
Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Upper Interrupts Setup Time* (IR8-5)	t_{UIRS}	−1	30			35	35	Note 2	ns min
		−2	25			30	30		
Lower Interrupts Setup Time* (IR4-1)	t_{LIRS}	−1	20			25	25	Note 2	ns min
		−2	15			20	20		
Three-State (TTR) Setup Time*	t_{TSS}	−1, 2	10			15	15	Note 2	ns min
Three-State (TTR) Overlap Time (with Trap)*	t_{TSOV}	−1, 2	15			5	5	Note 2	ns max
Three-State (TTR) Disable Delay*	t_{TSE}	−1	20			25	25	Notes 2, 4	ns max
		−2	15			20	20		
Idle-to-Three-State Enable Delay*	t_{IDL3}	−1	20			25	25	Notes 2, 4	ns max
		−2	15			20	20		
Trap (TTR) Overlap Time (with Three-State)	t_{TROV}	−1, 2	10			10	10	Notes 2, 4	ns max
Trap (TTR) to Address Delay*	t_{TRAD}	−1	60			70	70	Notes 2, 4	ns max
		−2	45			55	55		

NOTES
*Indicates that a limit for this parameter has changed from REV. A.
[1]T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).
[2]Input levels are GND and +3.0V; V_{DD} = +4.5V. Rise times are 5ns. Input timing reference levels and output reference levels are measured at +1.5V except for three-state reference levels, which are shown in Figure 2.
[3]Transitions measured per Figure 2.
[4]Address delays may be derated from the specified 50pF test loading by adding 7ns/50pF for increased capacitive loading.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	D7	25	Y6
2	D8	26	Y5
3	D9	27	Y4
4	D10	28	Y3
5	D11	29	Y2
6	D12	30	Y1
7	D13	31	Y0
8	D14	32	I0
9	D15	33	I1
10	EXIR1	34	I2
11	EXIR2	35	I3
12	GND	36	I4
13	EXIR3	37	V_{DD}
14	EXIR4	38	I5
15	TTR	39	I6
16	Y15	40	FLAG
16	Y14	41	CLK
18	Y13	42	D0
19	Y12	43	D1
20	Y11	44	D2
21	Y10	45	D3
22	Y9	46	D4
23	Y8	47	D5
24	Y7	48	D6

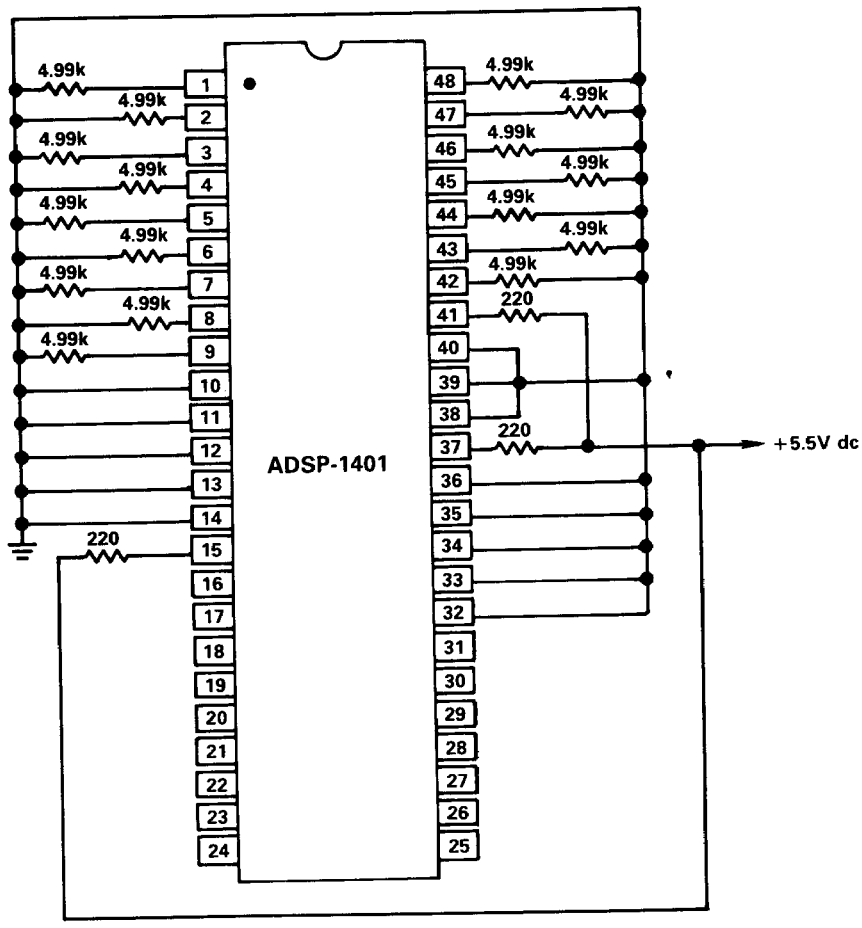
REV. B

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



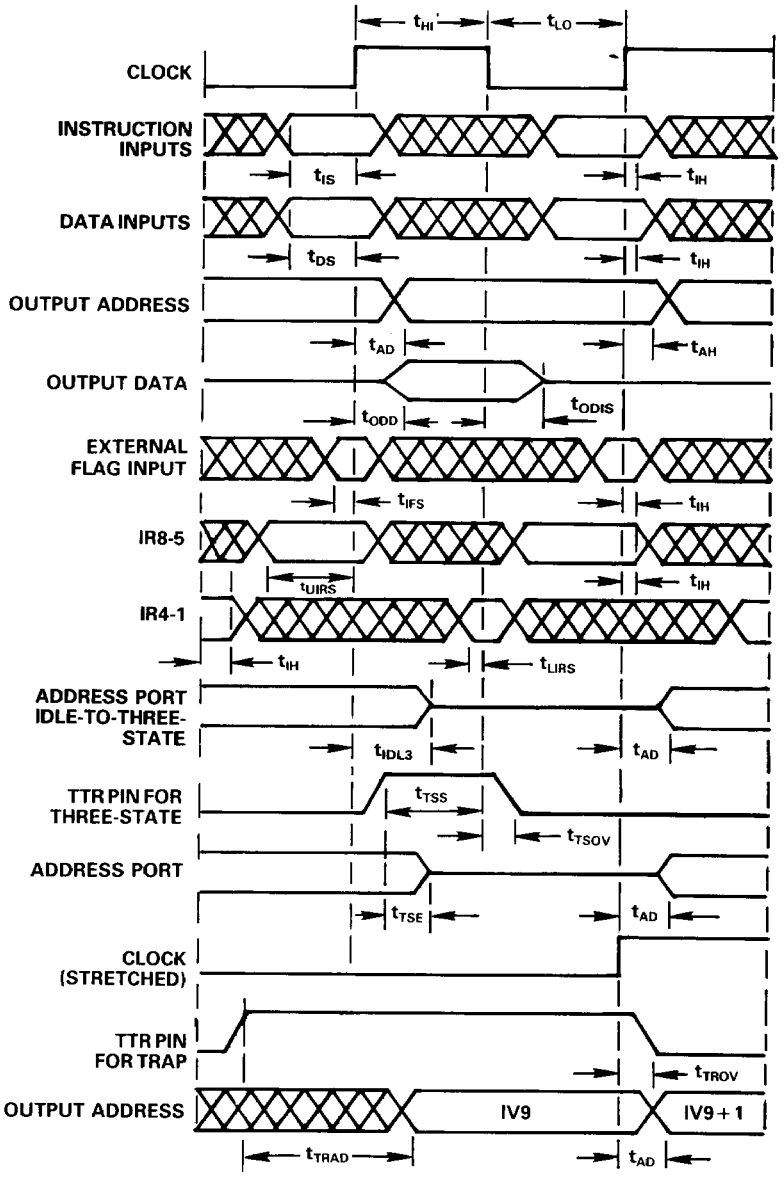


Figure 1. ADSP-1401 Timing Diagram

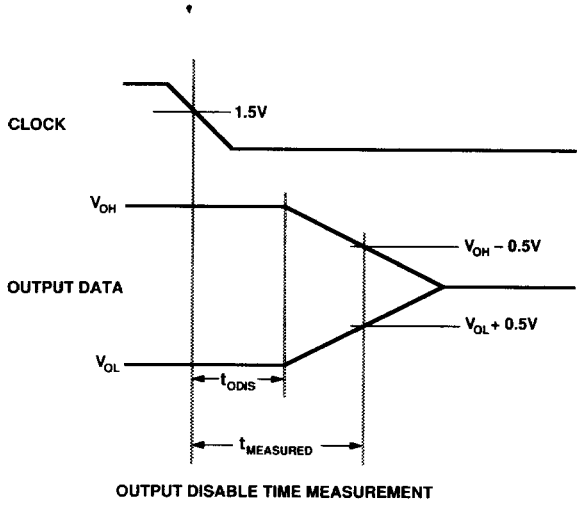


Figure 2. Three-State Reference Levels

Output disable time is measured from the time CLK reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{ODIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

REV. B

Mnemonic	Opcode (I_{6-0})	Description
Jump and Branch Instructions:		
JPCOF	001 0101	IF FLAG: JUMP PC (*self*)
JPCNF	011 0101	IF NOT FLAG: JUMP PC (*self*)
JTWO	101 cc01	IF COND: JUMP PC+2 (*skip*)
JDA	111 cc11	IF COND: JUMP DATA, ABSOLUTE
JDR	111 cc01	IF COND: JUMP DATA, RELATIVE
JDI	101 cc10	IF COND: JUMP DATA, INDIRECT
JDRST	100 11ii	IF SIGN OF C_i: JUMP DATA, $C_i <= R_i$; ELSE, $C_i <= C_i - 1$
*JRC	110 ccii	IF COND: JUMP R_i
JRS	110 11ii	IF SIGN OF C_i: JUMP R_i, $C_i <= C_i - 1$
JSA	111 cc00	IF COND: JUMP SUB, ABSOLUTE
JSR	111 cc10	IF COND: JUMP SUB, RELATIVE
RTN	101 cc11	IF COND: RETURN FROM SUB
*BRANCH	100 ccii	IF SIGN OF C_i: JUMP R_i; ELSE, $C_i <= C_i - 1$, IF COND: JUMP DATA
Stack Operations:		
Subroutine Stack		
PSDSS	001 1110	PUSH DATA ONTO SS
PPSSD	011 1110	POP SS TO DATA PORT
WRSSP	000 1110	WRITE SSP
RDSSP	010 1100	READ SSP
DSSP	000 0010	DECREMENT SSP
Register Stack		
SGSP	000 0111	SELECT GSP
SLSP	000 0110	SELECT LSP
RDRSP	010 1111	READ RSP
WRRSP	000 1100	WRITE RSP
PSPC	010 0011	PUSH PC ONTO RS
PSGSP	000 0101	PUSH GSP ONTO SS
PPGSP	000 0100	POP GSP FROM SS
PSDRS	001 1111	PUSH DATA ONTO RS
PPRSD	011 1111	POP RS TO DATA PORT
AIRSP	010 10ii	ADD i TO RSP
S1RSP	000 1111	SUBTRACT 1 FROM RSP
S4RSP	011 1100	SUBTRACT 4 FROM RSP
Status Register Operations:		
RDSR	010 1110	READ SR
WRSR	001 1100	WRITE SR
PSSR	010 0001	PUSH SR ONTO SS
PPSR	010 0010	POP SR FROM SS
Counter Operations:		
WRCNTR	011 10ii	WRITE C_i
CLRS	001 0100	CLEAR SIGN BIT
SETS	011 0100	SET SIGN BIT
PSCNTR	000 10ii	PUSH C_i ONTO SS
PPCNTR	001 10ii	POP C_i FROM SS
DCCNTR	011 00ii	DECREMENT C_i
IFCDEC	101 cc00	IF COND: DECREMENT C_0
Interrupt Control:		
CCIR	001 0001	CLEAR CURRENT INTERRUPT
CAIR	000 0001	CLEAR ALL INTERRUPTS
RTNIR	000 0011	RETURN FROM INTERRUPT
RDIV	010 1101	READ INTERRUPT VECTOR AND INCREMENT IVP
WRIV	000 1101	WRITE INTERRUPT VECTOR AND INCREMENT IVP
IRMBC	001 0011	IR MASK BITWISE CLEAR
IRMBS	001 0010	IR MASK BITWISE SET
DISIR	001 0110	DISABLE INTERRUPTS
ENAIR	011 0110	ENABLE INTERRUPTS
SLIR	001 0111	SELECT LATCHED INTERRUPTS
STIR	011 0111	SELECT TRANSPARENT INTERRUPTS
SLRIVP	001 1101	WRITE SLR<=D_{5-2} AND IVP<=D_{15-12}
Relative Address Width Controls:		
REL16	010 0100	SELECT 16-BIT RELATIVE ADDRESSING
REL12	010 0111	SELECT 12-BIT RELATIVE ADDRESSING
REL8	010 0110	SELECT 8-BIT RELATIVE ADDRESSING
Miscellaneous Instructions:		
CONT	000 0000	CONTINUE
IDLE	001 0000	IDLE
IHC	010 0101	ENABLE INSTRUCTION HOLD CONTROL
WCS	010 0000	WRITE CONTROL STORE

The SIGN condition is precluded from instructions prefixed with "*."

Table 2. ADSP-1401 Instruction Set

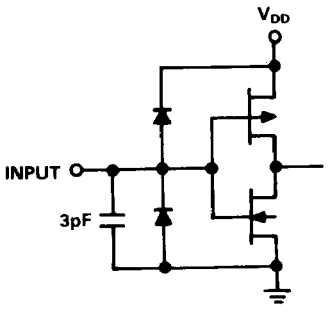


Figure 3. Equivalent Input Circuit

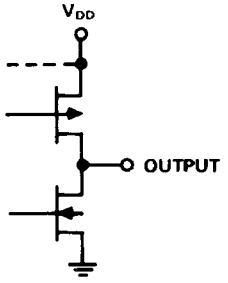


Figure 4. Equivalent Output Circuit

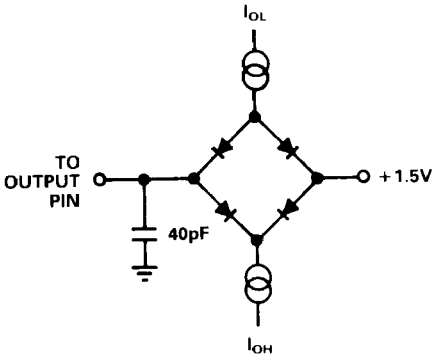


Figure 5. Normal Load for AC Measurements