DAC-8212

DUAL 12-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- **Two Matched 12-Bit DACs on One Chip**
- **Direct Parallel Load of All 12 Bits for High DataThroughput**
- **On-Chip Latches for Both DACs**
- **12-Bit Endpont Linearity (±1/2 LSB)**
- **+5V to +15V Single Cupply Operation**
- **DACs Matched to 1%**
- **Four-Quadrant Multiplication**
- **Low Power Consumption**
- **Available in Die Form**

APPLICATIONS

- **Automatic Test Equipment**
- **Robotics**
- **Programmable Instrumentation Equipment**
- **Digital Gain/Attenuation Control**
- **Ideal for Battery-Operated Equipment**

ORDERING INFORMATION†

		PACKAGE		
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE −55°C to +125°C	INDUSTRIAL TEMPERATURE −25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±2 LSB	DAC8212AV	DAC8212EV	DAC8212GP
±1 LSB	±4 LSB	DAC8212BV	DAC8212FV	DAC8212HP
±1 LSB	±4 LSB	—	—	DAC8212HPC††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

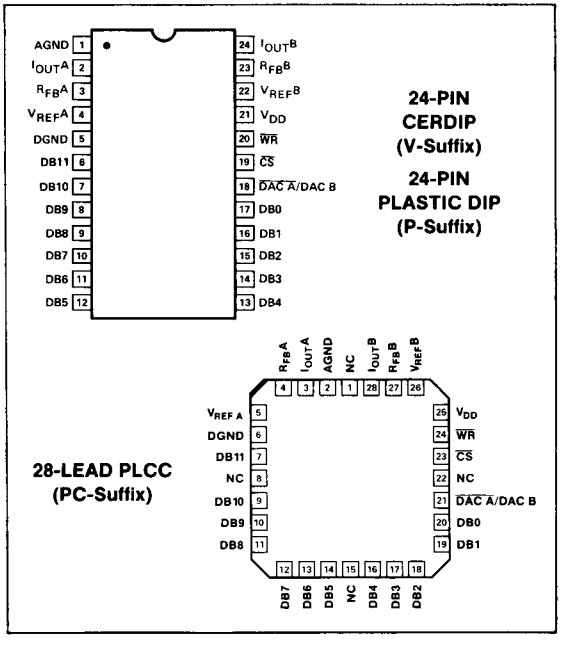
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

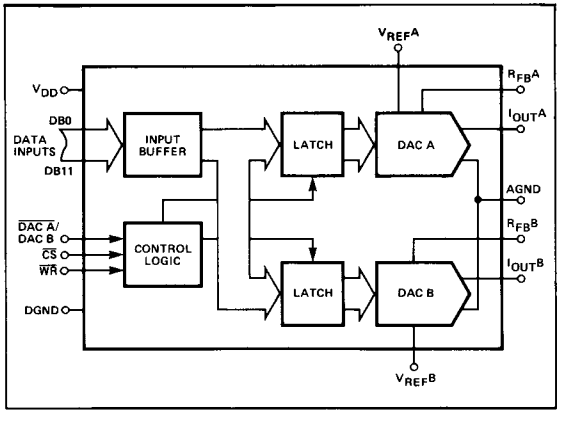
The DAC-8212 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8212 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8212 can operate on a single supply from +5V to +15V. Maximum power dissipation with CMOS logic levels and a +5V supply is less than 0.5mW. The DAC-8212 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic low, the input data latches are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A}$/DAC B control input.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... –0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
$I_{OUT}A$, $I_{OUT}B$ to AGND ..... –0.3V, V_{DD} +0.3V
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V
Operating Temperature Range
AV, BV Versions ..... –55°C to +125°C
EV, FV Versions ..... –25°C to +85°C
GP, HP, HPC Versions ..... –0°C to +70°C
Junction Temperature ..... +150C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (V)	57	10	°C/W
24-Pin Plastic DIP (P)	54	27	°C/W
28-Contact PLCC (PC)	66	29	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for PLCC package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

at V_{DD} = +5V or +15V, $V_{REF}A$ = $V_{REF}B$ = +10V, $V_{OUT}A$ = $V_{OUT}B$ = 0V; AGND = DGND = 0V; T_A = –55°C to +125°C apply for DAC-8212AV/BV; T_A = –25°C to +85°C apply for DAC-8212EV/FV; T_A = 0°C to +70°C apply for DAC-8212GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B.

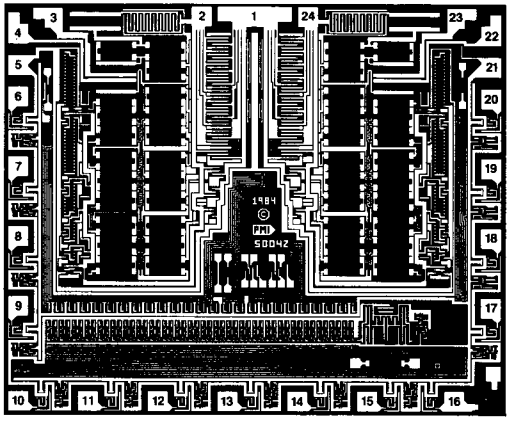
PARAMETER	SYMBOL	CONDITIONS		DAC-8212 MIN	DAC-8212 TYP	DAC-8212 MAX	UNITS
STATIC ACCURACY		Specifications apply to both DAC A and DAC B					
Resolution	N			12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8212A/E/G	—	—	±1/2	LSB
			DAC-8212B/F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic		—	—	±1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	T_A = +25°C	DAC-8212A/E/G	—	—	±2	LSB
			DAC-8212B/F/H	—	—	±4	
		T_A = Full Temp. Range	DAC-8212A/E/G	—	—	±3	
			DAC-8212B/F/H	—	—	±6	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)		—	±2	±5	ppm/°C
Output Leakage Current $I_{OUT}A$ (Pin 2), $I_{OUT}B$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C	—	±5	±50	nA
			T_A = Full Temp. Range	—	—	±100	
Input Resistance ($V_{REF}A$, $V_{REF}B$)	R_{REF}			8	11	15	kΩ
($V_{REF}A$/$V_{REF}B$) (Input Resistance Match)	$\Delta V_{REF}A$, B			—	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5V		2.4	—	—	V
		V_{DD} = +15V		13.5	—	—	
Digital Input Low	V_{INL}	V_{DD} = +5V		—	—	0.8	V
		V_{DD} = +15V		—	—	1.5	
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} and V_{INL} or V_{INH}	T_A = +25°C	—	±.001	±1	μA
			T_A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 2)	C_{IN}	DB0—DB11		—	—	10	pF
		$\overline{WR}$, $\overline{CS}$, DAC A/DAC B		—	—	15	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, $V_{OUT}A = V_{OUT}B$ = 0V; AGND = DGND = 0V; T_A = −55°C to +125°C apply for DAC-8212AV/BV; T_A = −25°C to +85°C apply for DAC-8212EV/FV; T_A = 0°C to +70°C apply for DAC-8212GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8212 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Notes 2, 3)						
Chip Select to Write Set-Up Time	t_{CS}		230	—	—	ns
Chip Select to Write Hold Time	t_{CH}		30	—	—	ns
DAC Select to Write Set-Up Time	t_{AS}		230	—	—	ns
DAC Select to Write Hold Time	t_{AH}		30	—	—	ns
DAC Select Set-Up Write Time	t_{DSS}		0	—	—	ns
Data Valid to Write Set-Up Time	t_{DS}		230	—	—	ns
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns
Write Pulse Width	t_{WR}		230	—	—	ns
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	2	mA
		All Digital Inputs 0V or V_{DD}	—	10	100	µA
DC Supply Rejection (ΔGain/ΔV_{DD})	PSR	ΔV_{DD} = ±5%	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{pD}	T_A = +25°C	—	—	300	ns
Current Settling Time (Notes 5, 6)	t_s	T_A = +25°C	—	—	1	µs
Output Capacitance	$C_{OUT}A$	DAC Latches Loaded	—	—	90	pF
	$C_{OUT}B$	with 0000 0000 0000	—	—	90	
	$C_{OUT}A$	DAC Latches Loaded	—	—	120	
	$C_{OUT}B$	with 1111 1111 1111	—	—	120	
AC Feedthrough at $I_{OUT}A$ or $I_{OUT}B$	FT_A	$V_{REF}A$ to $I_{OUT}A$; $V_{REF}A$ = $20V_{p-p}$, f = 100kHz; T_A = +25°C	—	—	−70	dB
	FT_B	$V_{REF}B$ to $I_{OUT}B$; $V_{REF}B$ = $20V_{p-p}$, f = 100kHz; T_A = +25°C	—	—	−70	

NOTES:
1. Measured using internal $R_{FB}A$ and $R_{FB}B$. Both DAC digital inputs = 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
2. Guaranteed and not tested.
3. See timing diagram.
4. From 50% of digital input to 90% of final analog output current. $V_{REF}A = V_{REF}B$ = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
5. $\overline{WR}$, $\overline{CS}$ = 0V; DB0—DB11 = 0V to V_{DD} or V_{DD} to 0V.
6. Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
7. Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.

DICE CHARACTERISTICS



DIE SIZE 0.137 × 0.114 inch, 15,618 sq. mils
(3.48 × 2.90mm, 10.10 sq. mm)

1. AGND
2. $I_{OUT}A$
3. $R_{FB}A$
4. $V_{REF}A$
5. DGND
6. DB11
7. DB10
8. DB9
9. DB8
10. DB7
11. DB6
12. DB5
13. DB4
14. DB3
15. DB2
16. DB1
17. DB0
18. $\overline{DAC\ A/DAC\ B}$
19. $\overline{CS}$
20. $\overline{WR}$
21. V_{DD}
22. $V_{REF}B$
23. $R_{FB}B$
24. $I_{OUT}B$

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, $V_{OUT}A = V_{OUT}B$ = 0V; AGND = DGND = 0V; T_A = 25°C.

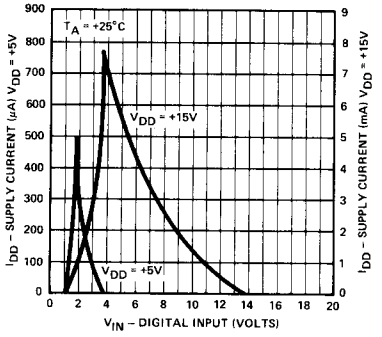
PARAMETER	SYMBOL	CONDITIONS	DAC-8212G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	(Note 1)	±1	LSB MAX
Full Scale Gain Error (Note 2)	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage ($I_{OUT}A$, $I_{OUT}B$)	I_{LKG}	Digital Inputs = 0000 0000 0000 Pad 2 and 24	±50	nA MAX
Input Resistance ($V_{REF}A$, $V_{REF}B$)	R_{REF}	Pad 4 and 22	8/15	kΩMIN/ kΩMAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\Delta V_{REF}A, B$		±1	% MAX
Digital Input High	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = +5V V_{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}; V_{INL} or V_{INH}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSR	ΔV_{DD} = ±5%	0.002	%/% MAX

NOTES:
1. All grades are monotonic.
2. Measured using internal $R_{FB}A$ and $R_{FB}B$.

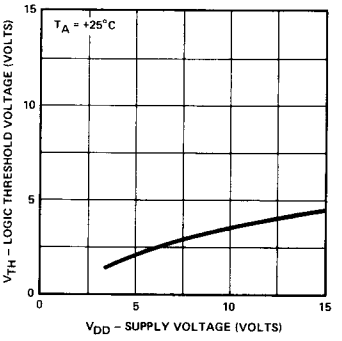
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

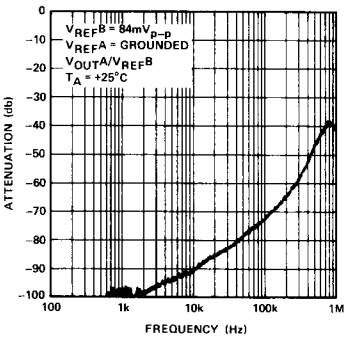
SUPPLY CURRENT vs LOGIC LEVEL



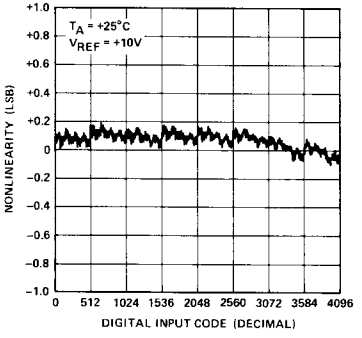
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



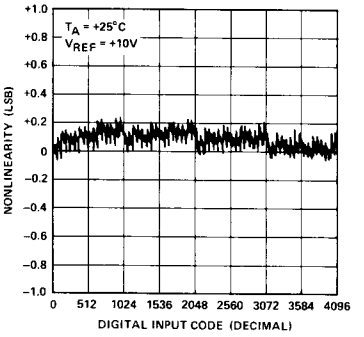
ANALOG CROSSTALK vs FREQUENCY



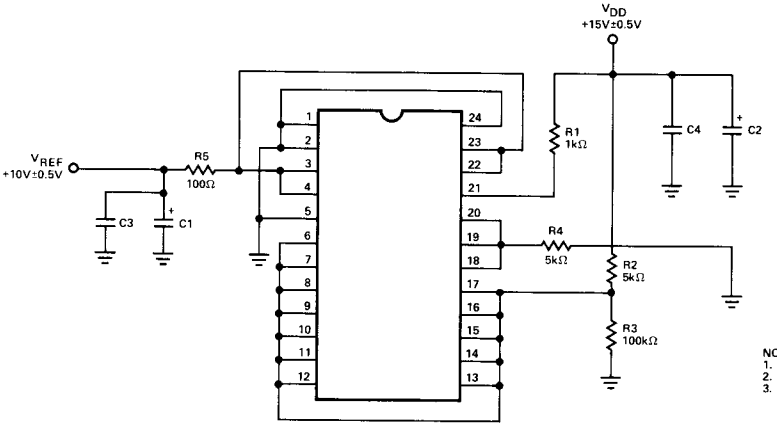
NONLINEARITY vs DIGITAL CODE (V_{DD} = +5V)



NONLINEARITY vs DIGITAL CODE (V_{DD} = +15V)

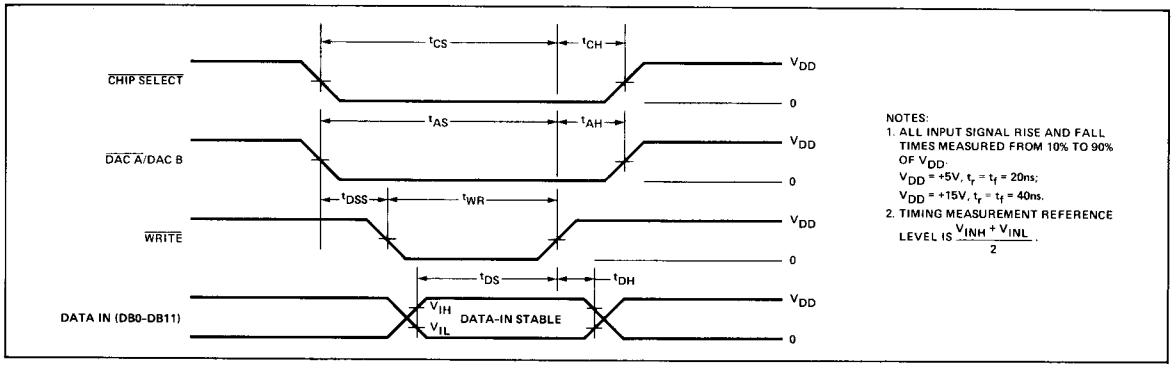


BURN-IN CIRCUIT



NOTES:
1. C1 = C2 4.7μF TANTALUM, 50V DC; EVERY 10TH DEVICE.
2. C3 = C4 0.01μF CERAMIC, 50V DC; EVERY 10TH DEVICE.
3. ALL MATERIAL TO WITHSTAND 150°C.

WRITE CYCLE TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

INTEGRAL NONLINEARITY (INL) OR NONLINEARITY (NL)

This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points, expressed as a percent of full-scale range or in terms of LSBs.

For DACs, a specification of ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum differential nonlinearity.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. Maximum DNL error is less than or equal to twice the maximum INL.

GAIN ERROR (G_{FSE})

The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

SETTLING TIME

Settling time is the elapsed time for the analog output to reach its final value within a specified error band after a digital input code change. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band.

PROPAGATION DELAY

This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output-current reaching 90% of its final value.

OUTPUT CAPACITANCE

Output capacitance is that capacitance between $I_{OUT}A$, $I_{OUT}B$, and AGND.

A.C. FEEDTHROUGH

The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of a single DAC. R is typically 11kΩ. Figure 2 gives an approximate equivalent switch circuit.

The binary-weighted currents are switched between I_{OUT} and AGND by N-channel MOS transistor switches. This maintains a constant current in each ladder leg independent of switch state. It is important that both N-channel switch "ON" resistances be matched so that the linearity errors can be kept at a minimum.

FIGURE 1: Simplified D/A Circuit

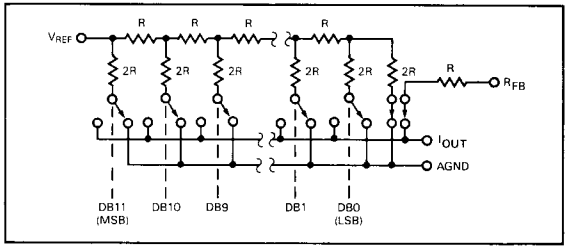
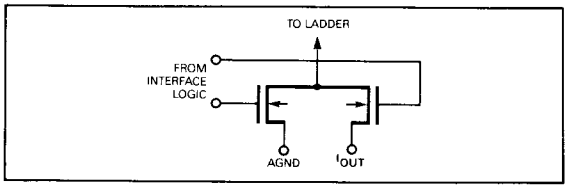


FIGURE 2: N-Channel Current Steering Switch



This also dictates that the voltage difference between I_{OUT} and AGND terminals be as close to zero as practical. This is easily accomplished by tying AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The op amp feedback can then be tied directly to the R_{FB} terminal of the DAC; this will close the loop. The op amp, then, serves a two-fold function: it maintains the voltage difference between the DAC output terminals at virtual zero volts, and performs the current-to-voltage conversion for the DAC's output current. The output voltage is then dependent on the digital input code.

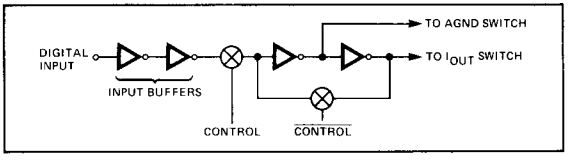
Input resistance at V_{REF} (Figure 1) is always equal to R-LDR (R-LDR is the R/2R resistor ladder characteristic resistance and is equal to value "R"). Since the input resistance at V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or current, AC or DC, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} resistor is recommended to define scale factor).

The capacitance at I_{OUT} terminal, C_{OUT}, is code dependent and varies from 90pF (all digital inputs at AGND) to 120pF (all digital inputs HIGH).

DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

FIGURE 3: Digital Input Structure



The input buffers are simple CMOS inverters designed such that when the DAC-8212 is operated with $V_{DD} = +5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

When the digital inputs are in the region of 1.2 to 2.8V with a +5V power supply, or 1.2 to 13.5V with a +15V power supply, the input buffers operate in their linear region and draw current from the power supply. It is, therefore, recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible to keep supply currents at a minimum. The DAC-8212 may be operated with any supply voltage in the range $+5V \leq V_{DD} \leq +15V$. The input logic levels are CMOS compatible (1.5V and 13.5V) at $V_{DD} = +15V$.

BASIC APPLICATIONS

UNIPOLAR OUTPUT CIRCUIT

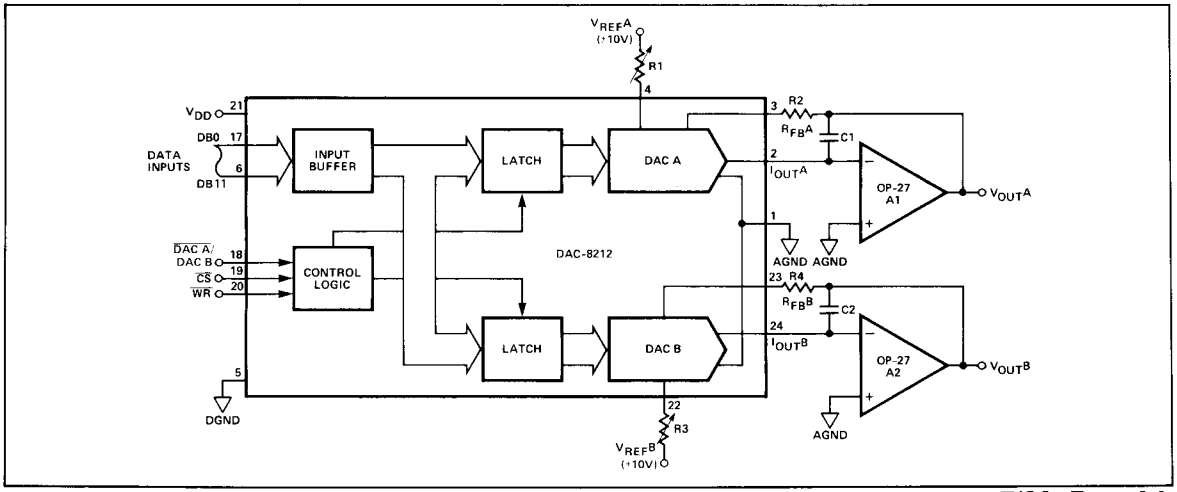
Figure 4 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8212, and Table 1 shows the code table. Resistors R1, R2, and R3, R4, are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = +10V$ is

TABLE 1: Unipolar Binary Code Table (Refer to Figure 4)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE:
1 LSB = $(2^{-12})(V_{REF}) = \frac{1}{4096}(V_{REF})$

FIGURE 4: Dual DAC Unipolar Operation (2-Quadrant Multiplication)



0.048%, and 0.097% for the low grade device. See Table 3 for recommended values if using these resistors. Full-scale output voltage = V_{REF} −1 LSB = $V_{REF} \times (1 - 2^{-12})$ or $V_{REF} \times (4095/4096)$ with all digital inputs high. Low temperature coefficient (approximately 50ppm/°C) resistor or trimmers should be used. Full-scale can also be adjusted by varying V_{REF} voltage.

BIPOLAR OUTPUT CIRCUIT

Figure 5 shows how the DAC-8212 can be configured to operate in the bipolar mode (4-quadrant multiplication), and Table 2 shows the code table. As with the unipolar circuit of Figure 4, resistors R1, R2, and R3, R4, are used only if full-scale gain adjustment is required. Table 3 gives recommended values. R1 and R3 are used to adjust for zero voltage at the output of DAC A or DAC B respectively. The voltage is adjusted with the digital inputs set to 1000 0000 0000 for DAC A or DAC B. Matching and tracking is essential for resistor pairs R6, R7, and R9, R10. Capacitors C1 and C2 (10—15pF) provide phase compensation; they are required if using high speed op amps to prevent ringing or oscillations.

To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244μV) over the operating temperature range.

PROGRAMMABLE WINDOW DETECTOR

Figure 6 shows the DAC-8212 used in a programmable window detector. The required upper and lower limits for the test are loaded into DAC A and DAC B. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero.

TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 5)

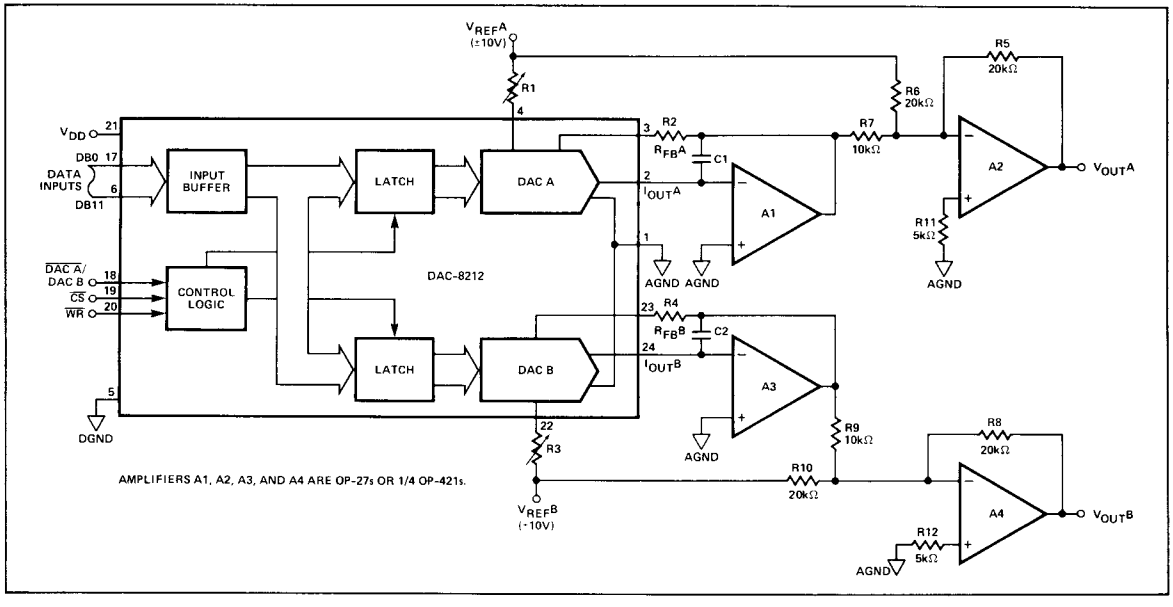
BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTE:
1 LSB = (2^{-11}) $(V_{REF}) = \frac{1}{2048}(V_{REF})$

TABLE 3: Recommended Trim Resistor Values vs Grade for Figures 4 and 5

TRIM RESISTOR	BV/FV/HP	AV/EV/GP
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

FIGURE 5: Dual DAC Bipolar Operation (4-Quadrant Operation)



APPLICATION HINTS

GROUND MANAGEMENT

Transient voltages between AGND and DGND can appear as noise at the DAC-8212's output. Figure 7 shows all analog grounds tied together and one connection from digital ground to analog ground. Note that AGND and DGND take off on their own ground paths, i.e., power grounds are kept separate from analog grounds. DGND pin is the return for supply currents and serves as the reference point for the digital inputs. Thus, DGND should be connected to the same ground as the circuitry which drives the digital inputs. AGND is the high-quality analog ground connection; this pin should serve as the reference point for all analog ground connections. It is recommended that any analog signal path carrying significant currents have its own return connection as shown in Figure 7.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC-8212 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with a 0.1μF ceramic is highly recommended. The decoupling capacitors should be connected between the DAC-8212 supply pin (V_{DD}) and AGND pin.

WRITE ENABLE TIMING

During the period when both $\overline{CS}$ and $\overline{WR}$ are held low, the selected DAC latch is transparent and its analog output responds directly to the data on the data bus line, DB0—DB11. Unwanted variations may appear at the input, therefore, the $\overline{WR}$ line should not go low until the data bus is fully settled (DATA VALID).

FIGURE 7: Recommended Ground Connections

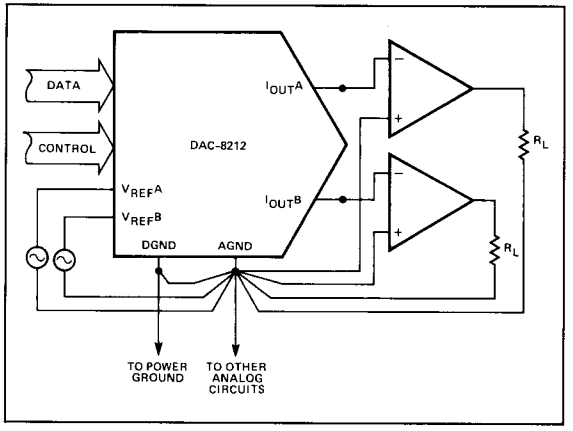
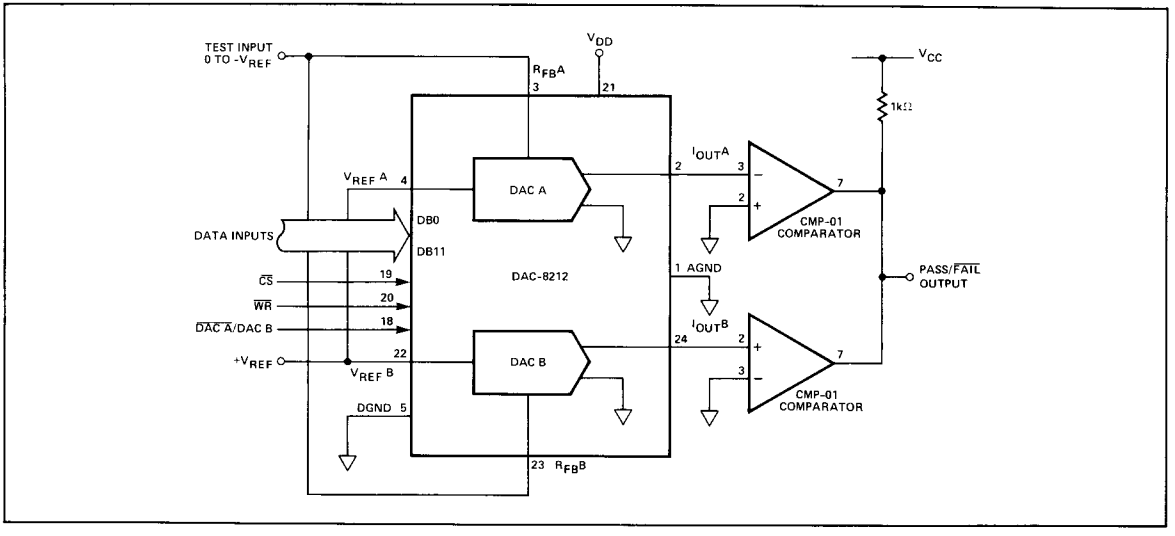


FIGURE 6: Digitally-Programmable Window Detector (Upper and Lower Limit Detector)



MICROPROCESSOR INTERFACE

Interfacing to an 8-bit or 16-bit bus system has been simplified by the loading structure versatility of the DAC-8212. Data loading into its 12-bit wide data latch is simplified by the use of only two control signals, $\overline{CS}$ and $\overline{WR}$.

8-BIT MICROPROCESSORS

8085A Microprocessor Interface: Loading data into the DAC-8212's 12-bit wide latch from an 8-bit bus will require two write cycles from the microprocessor. Data occupies two adjacent locations in the microprocessor's memory; several formats are possible and depends on the one desired. One scheme for interfacing the DAC-8212 to the 8085A 8-bit microprocessor is shown in Figure 8. Four MSBs are latched into the 74LS75 latch in the first cycle, and the entire 12-bit word is then loaded into the DAC-8212's data latch on the next write cycle. An alternate scheme would be to use an 8-bit latch so that the user can load the lower order bits in the first cycle. The 74LS139 is a dual 1 of 4 address decoder that supplies control signals for DAC selection, $\overline{CS}$, high byte, and low byte. The NAND gate and inverter provides a constant chip select active-low signal while allowing the decoder to select either DAC A or DAC B.

6800 Microprocessor Interface: Because the DAC-8212 has a versatile data bus structure, interfacing it to the 6800 microprocessor is simplified and similar to that of the 8085A microprocessor circuit above. The circuit is shown in Figure 9.

16-BIT MICROPROCESSORS

Figures 10 and 11 show the DAC-8212's interface schemes for the 8086 and 68000 16-bit microprocessors. Circuit simplicity is achieved by connecting the DAC's data bus directly to the microprocessor. The 12-bit wide word is written to the DAC in one MOV instruction. The address decoder provides the DAC select and chip select signals and is programmed by the microprocessor.

FIGURE 8: DAC-8212 Dual DAC Interface with the 8085A 8-Bit Microprocessor

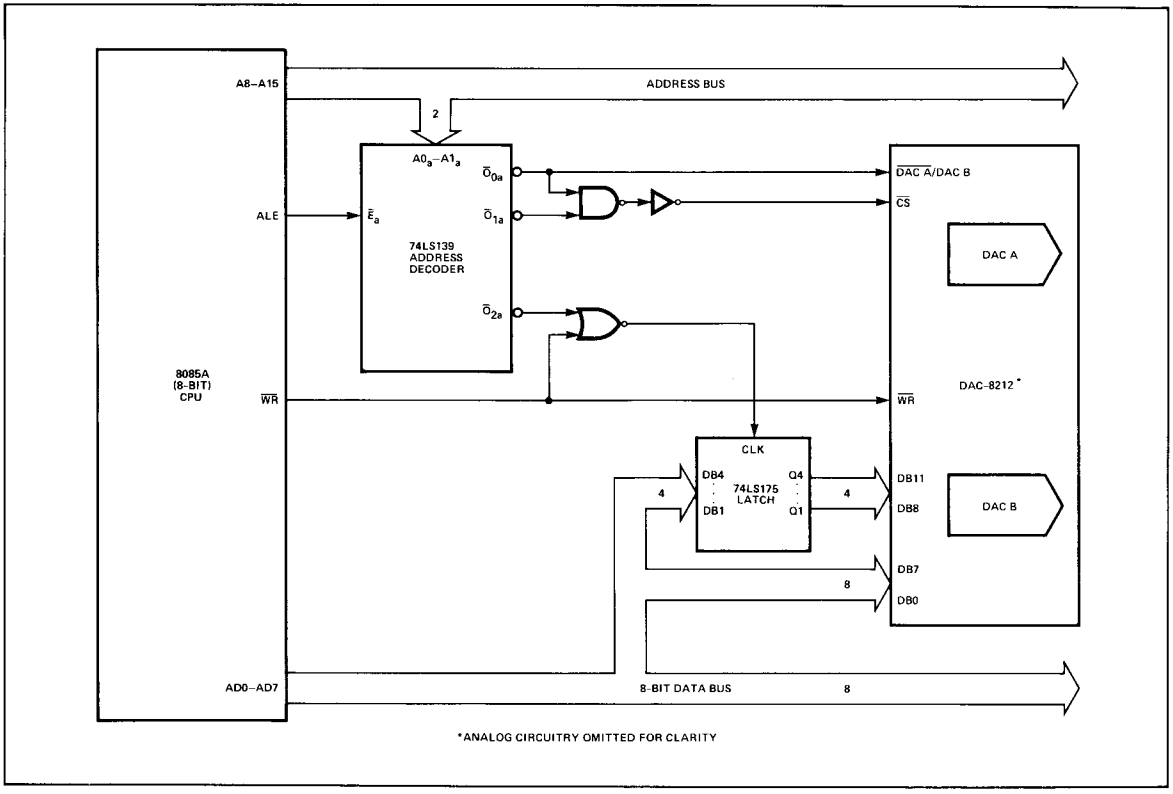


FIGURE 9: DAC-8212 Dual DAC Interface with the 6800 8-Bit Microprocessor

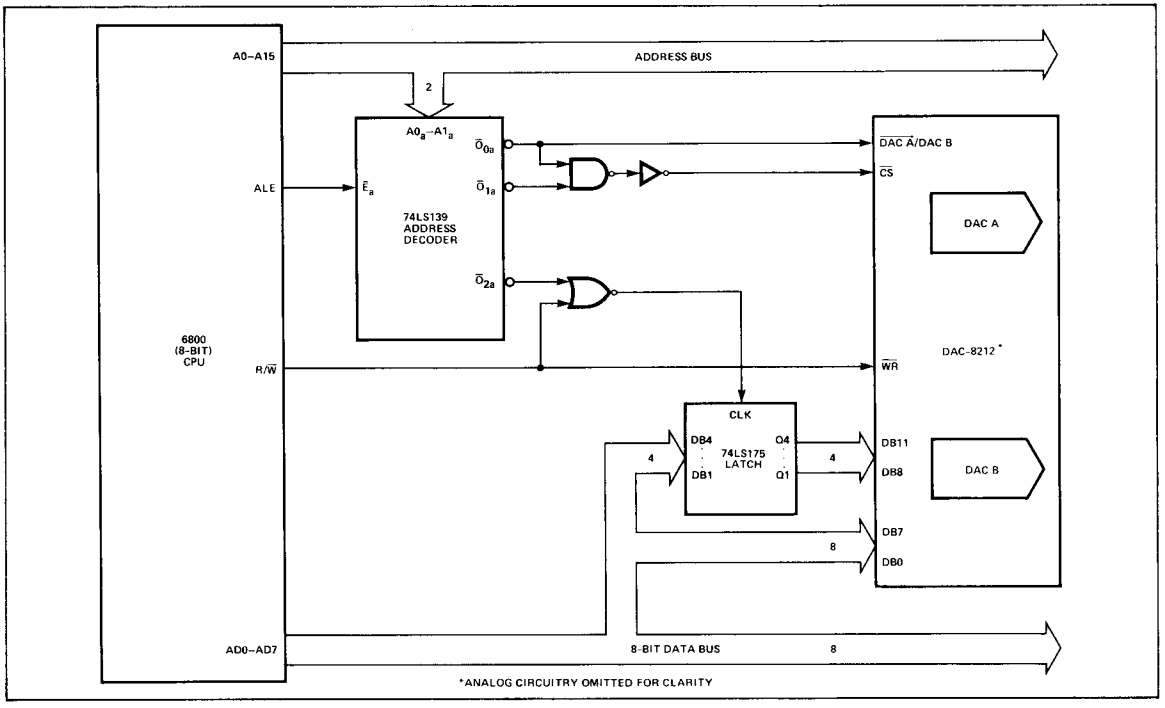


FIGURE 10: DAC-8212 Dual DAC Interface to the 8086 16-Bit Microprocessor

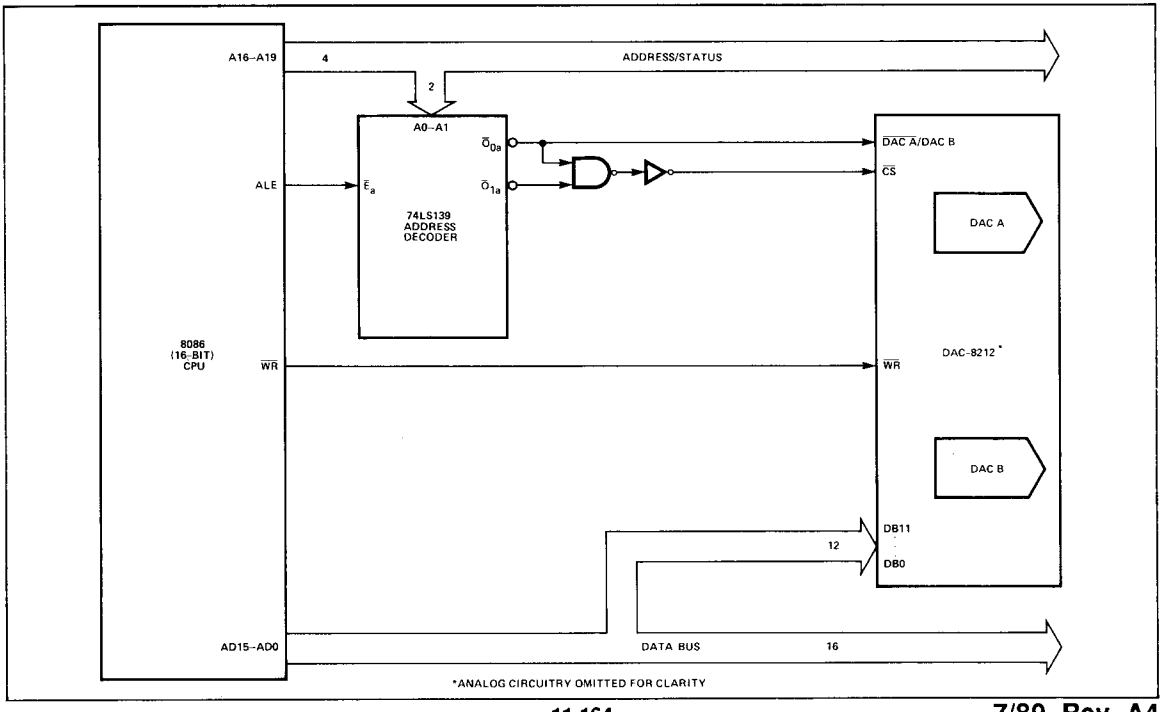


FIGURE 11: DAC-8212 Dual DAC Interface to the 68000 16-Bit Microprocessor