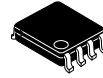


# LVDS Single Port High Speed Repeater

## FIN1101



SOIC8  
CASE 751EB



US8  
CASE 846AN

### General Description

This single port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. It accepts and outputs LVDS levels with a typical differential output swing of 330 mV which provides low EMI at ultra low power dissipation even at high frequencies. It can directly accept multiple differential I/O including: LVPECL, HSTL, and SSTL-2 for translating directly to LVDS.

### Features

- Up to 1.6 Gb/s Full Differential Path
- 3.5 ps Max Random Jitter and 135 ps Max Deterministic Jitter
- 3.3 V Power Supply Operation
- Wide Rail-To-Rail Common Mode Range
- Ultra Low Power Consumption
- LVDS Receiver Inputs Accept LVPECL, HSTL, and SSTL-2 Directly
- Power Off Protection
- 7 kV HBM ESD Protection (All Pins)
- Meets or Exceed the TA/EIA-644-A LVDS Standard
- Packaged in 8-Pin SOIC and US8
- Open Circuit Fail Safe Protection
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

### PIN DESCRIPTIONS

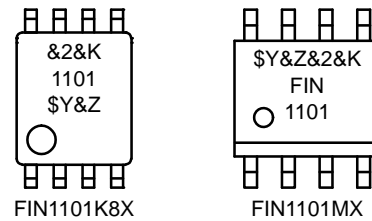
Pin Name	Description
R <sub>IN+</sub>	Non-Inverting LVDS Inputs
R <sub>IN-</sub>	Inverting LVDS Inputs
D <sub>OUT+</sub>	Non-Inverting Driver Outputs
D <sub>OUT-</sub>	Inverting Driver Outputs
EN	Driver Enable Pin
V <sub>CC</sub>	Power Supply
GND	Ground

### FUNCTION TABLE

Inputs			Outputs	
EN	R <sub>IN+</sub>	R <sub>IN-</sub>	D <sub>OUT+</sub>	D <sub>OUT-</sub>
H	H	L	H	L
H	L	H	L	H
H	Fail Safe Case		H	L
L	X	X	Z	Z

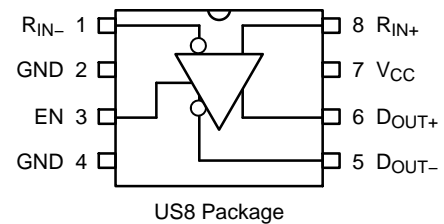
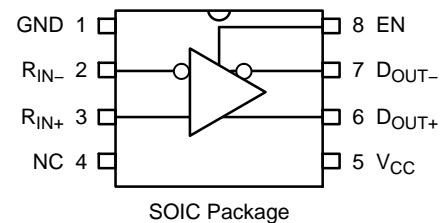
H = HIGH Logic Level      L = LOW Logic Level  
X = Don't Care                Z = High Impedance

### MARKING DIAGRAM

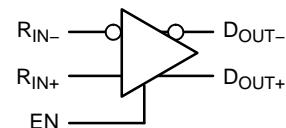


\$Y = Logo  
&Z = Assembly Plant Code  
&2 = 2-Digit Date Code  
&K = 2-Digits Lot Run Traceability Code  
1101, FIN1101 = Specific Device Code

### CONNECTION DIAGRAMS



### FUNCTIONAL DIAGRAM



### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5 V to +4.6 V
$V_{IN}$	LVDS DC Input Voltage	-0.5 V to +4.6 V
$V_{OUT}$	LVDS DC Output Voltage	-0.5 V to +4.6 V
$I_{OSD}$	Driver Short Circuit Current	Continuous 10 mA
$T_{STG}$	Storage Temperature Range	-65°C to +150°C
$T_J$	Max Junction Temperature	150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C
	ESD (Human Body Model)	7000 V
	ESD (Machine Model)	300 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value
$V_{CC}$	Supply Voltage	3.0 V to 3.6 V
$T_A$	Operating Temperature	-40°C to +85°C
$ V_{ID} $	Magnitude of Input Differential Voltage	100 mV to $V_{CC}$
$V_{IC}$	Common Mode Input Voltage	$(0\text{ V} +  V_{ID}  / 2)$ to $(V_{CC} -  V_{ID}  / 2)$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

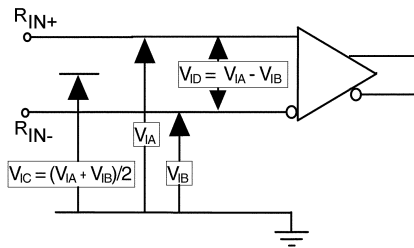
Symbol	Parameter	Test Conditions	Min	Typ (Note 1)	Max	Unit
$V_{TH}$	Differential Input Threshold HIGH	See Figure 1; $V_{IC} = +0.05\text{ V}, +1.2\text{ V},$ or $(V_{CC} - 0.05\text{ V})$	-	-	100	mV
$V_{TL}$	Differential Input Threshold LOW	See Figure 1; $V_{IC} = +0.05\text{ V}, +1.2\text{ V},$ or $(V_{CC} - 0.05\text{ V})$	-100	-	-	mV
$V_{IH}$	Input High Voltage (EN)		2.0	-	$V_{CC}$	V
$V_{IL}$	Input Low Voltage (EN)		GND	-	0.8	V
$V_{OD}$	Output Differential Voltage	$R_L = 100\ \Omega$ , Driver Enabled, See Figure 2	250	330	450	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change from Differential LOW-to-HIGH	$R_L = 100\ \Omega$ , Driver Enabled, See Figure 2	-	-	25	mV
$V_{OS}$	Offset Voltage	$R_L = 100\ \Omega$ , Driver Enabled, See Figure 2	1.125	1.23	1.375	V
$\Delta V_{OS}$	Offset Magnitude Change from Differential LOW-to-HIGH	$R_L = 100\ \Omega$ , Driver Enabled, See Figure 2	-	-	25	mV
$I_{OS}$	Short Circuit Output Current	$D_{OUT+} = 0\text{ V}$ & $D_{OUT-} = 0\text{ V}$ , Driver Enabled	-	-3.4	-6	mA
$I_{OS}$	Short Circuit Output Current	$V_{OD} = 0\text{ V}$ , Driver Enabled	-	$\pm 3.4$	$\pm 6$	mA
$I_{IN}$	Input Current (EN, $D_{INX+}$ , $D_{INX-}$ )	$V_{IN} = 0\text{ V}$ to $V_{CC}$ , Other Input = $V_{CC}$ or 0 V (for Differential Inputs)	-	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	Power-Off Input or Output Current	$V_{CC} = 0\text{ V}$ , $V_{IN}$ or $V_{OUT} = 0\text{ V}$ to 3.6 V	-	-	$\pm 20$	$\mu\text{A}$
$I_{CCZ}$	Disabled Power Supply Current	Drivers Disabled	-	3.2	5.5	mA
$I_{CC}$	Power Supply Current	Drivers Enabled, Any Valid Input Condition	-	9.3	13.5	mA
$I_{OZ}$	Disabled Output Leakage Current	Driver Disabled, $D_{OUT+} = 0\text{ V}$ to 3.6 V or $D_{OUT-} = 0\text{ V}$ to 3.6 V	-	-	$\pm 20$	$\mu\text{A}$
$V_{IC}$	Common Mode Voltage Range	$ V_{ID}  = 100\text{ mV}$ to $V_{CC}$	$0\text{ V} +  V_{ID}  / 2$	-	$V_{CC} - ( V_{ID}  / 2)$	V
$C_{IN}$	Input Capacitance	EN Input	-	2.2	-	pF
		Data Input	-	2.0	-	pF
$C_{OUT}$	Output Capacitance		-	2.6	-	pF

1. All typical values are at  $T_A = 25^\circ\text{C}$  and with  $V_{CC} = 3.3\text{ V}$ .

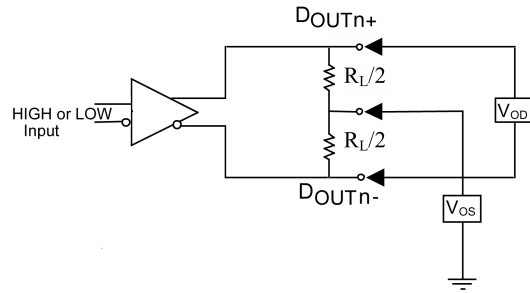
**AC ELECTRICAL CHARACTERISTICS** (Over supply voltage and operating temperature ranges, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Unit
t <sub>PLHD</sub>	Differential Propagation Delay LOW-to-HIGH	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF, V <sub>ID</sub> = 200 mV to 450 mV, V <sub>IC</sub> =  V <sub>ID</sub>   / 2 to (V <sub>CC</sub> - (V <sub>ID</sub> / 2)), Duty Cycle = 50%, See Figure 3 and Figure 4	0.75	1.1	1.75	ns
t <sub>PHLD</sub>	Differential Propagation Delay HIGH-to-LOW		0.75	1.1	1.75	ns
t <sub>TLHD</sub>	Differential Output Rise Time (20% to 80%)		0.29	0.40	0.58	ns
t <sub>THLD</sub>	Differential Output Fall Time (80% to 20%)		0.29	0.40	0.58	ns
t <sub>SK(P)</sub>	Pulse Skew  t <sub>PLH</sub> - t <sub>PHL</sub>		-	0.01	0.2	ns
t <sub>SK(PP)</sub>	Part-to-Part Skew (Note 3)		-	-	0.5	ns
f <sub>MAX</sub>	Maximum Frequency (Note 4) (Note 5)		400	800	-	MHz
t <sub>pZHD</sub>	Differential Output Enable Time from Z to HIGH	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF, See Figure 2 and Figure 3	-	2.1	5	ns
t <sub>pZLD</sub>	Differential Output Enable Time from Z to LOW		-	2.3	5	ns
t <sub>pHZD</sub>	Differential Output Disable Time from HIGH to Z		-	1.5	5	ns
t <sub>pLZD</sub>	Differential Output Disable Time from LOW to Z		-	1.8	5	ns
t <sub>DJ</sub>	LVDS Data Jitter, Deterministic	V <sub>ID</sub> = 300 mV, PRBS = 2 <sup>23</sup> - 1, V <sub>IC</sub> = 1.2 V at 800 Mbps	-	85	135	ps
t <sub>RJ</sub>	LVDS Clock Jitter, Random (RMS)	V <sub>ID</sub> = 300 mV V <sub>IC</sub> = 1.2 V at 400 MHz	-	2.1	3.5	ps

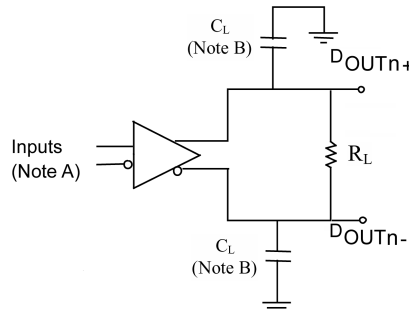
2. All typical values are at T<sub>A</sub> = 25°C and with V<sub>CC</sub> = 3.3 V, V<sub>ID</sub> = 300 mV, V<sub>IC</sub> = 1.2 V unless otherwise specified.
3. t<sub>SK(PP)</sub> is the magnitude of the difference in differential propagation delay times between identical channels of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.
4. Passing criteria for maximum frequency is the output V<sub>OD</sub> > 200 mV and the duty cycle is 45% to 55% with all channels switching.
5. Output loading is transmission line environment only; C<sub>L</sub> is < 1 pF of stray test fixture capacitance.



**Figure 1. Differential Receiver Voltage Definitions and Propagation I and Transition Time Test Circuit**



**Figure 2. Differential Driver DC Test Circuit**



Note A: All LVDS input pulses have frequency = 10 MHz, t<sub>R</sub> or t<sub>F</sub> ≤ 0.5 ns  
 Note B: C<sub>L</sub> includes all probe and test fixture capacitances

**Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit**

# FIN1101

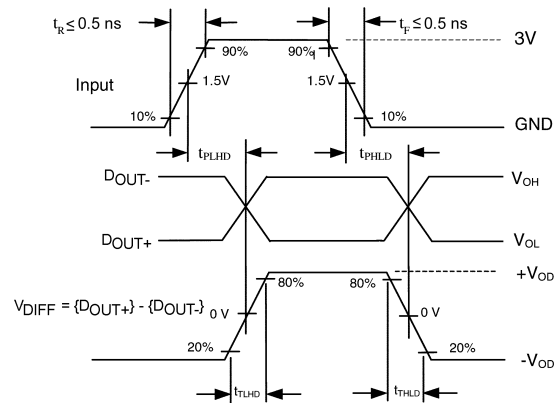
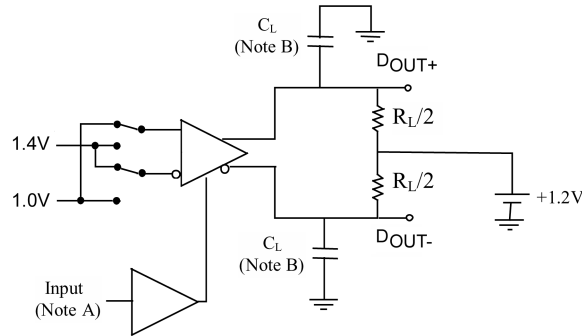


Figure 4. AC Waveforms



Note A: All LVTTTL input pulses have frequency = 10 MHz,  $t_R$  or  $t_F \leq 2$  ns  
 Note B:  $C_L$  includes all probe and test fixture capacitances

Figure 5. Differential Driver Enable and Disable Test Circuit

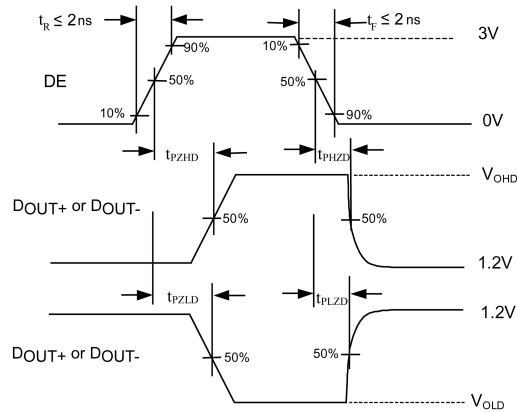


Figure 6. Enable and Disable AC Waveforms

## ORDERING INFORMATION

Order Number	Package Number	Package Description	Shipping†
FIN1101MX	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow (Pb-Free)	2500 / Tape & Reel
FIN1101K8X	MAB08A	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide (Pb-Free)	3000 / Tape & Reel

†For Information On Tape And Reel Specifications, Including Part Orientation And Tape Sizes, Please Refer To Our Tape And Reel Packaging Specifications Brochure, Brd8011/D.

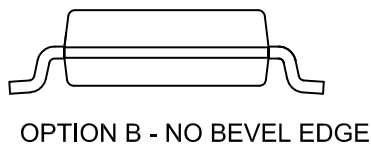
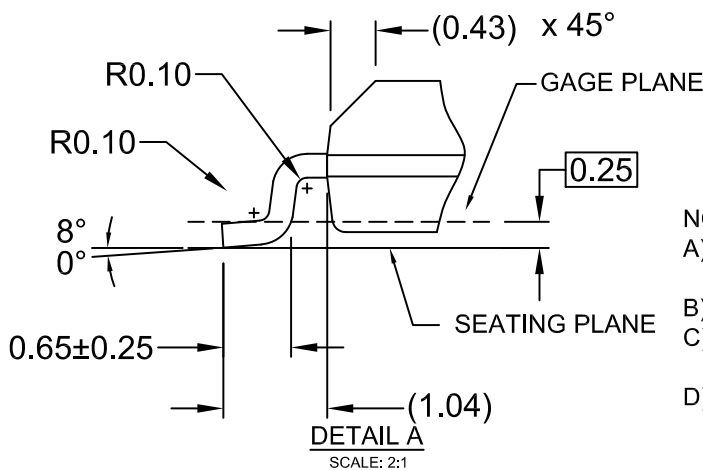
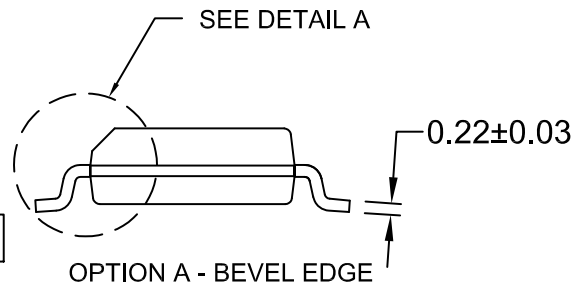
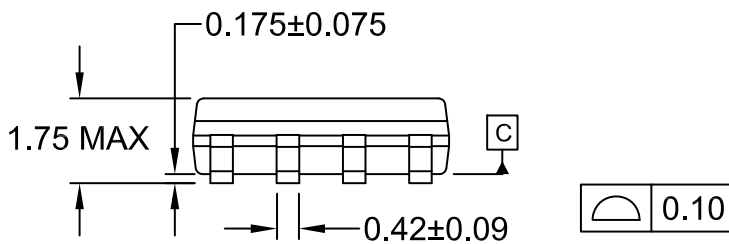
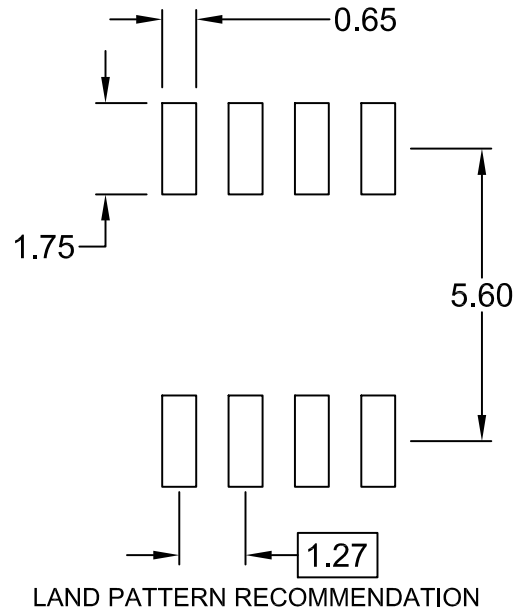
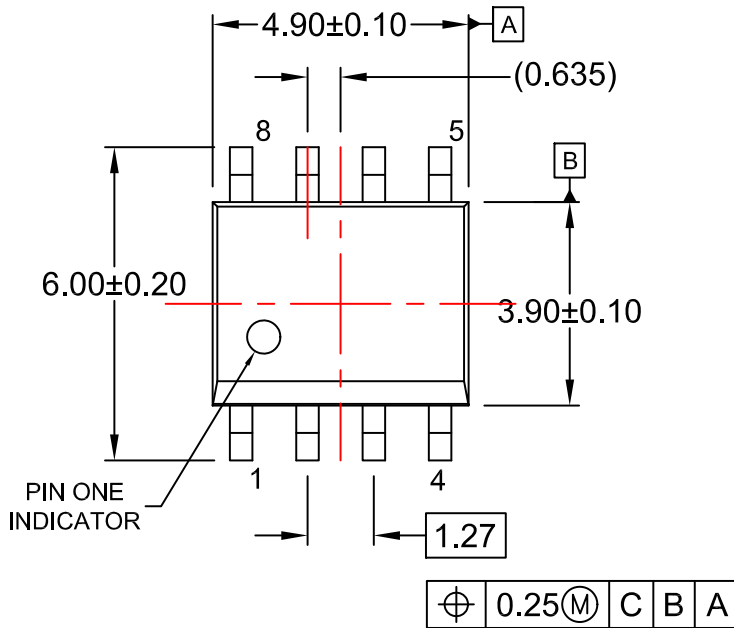
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

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**SOIC8**  
**CASE 751EB**  
**ISSUE A**

DATE 24 AUG 2017



- NOTES:  
 A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.  
 D) LANDPATTERN STANDARD: SOIC127P600X175-8M

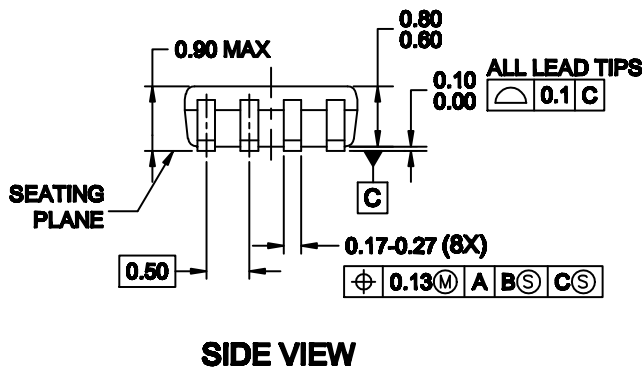
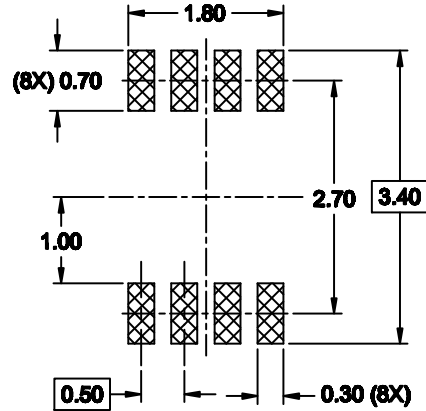
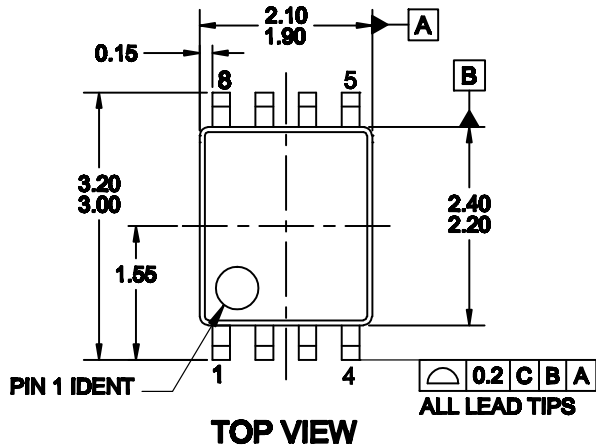
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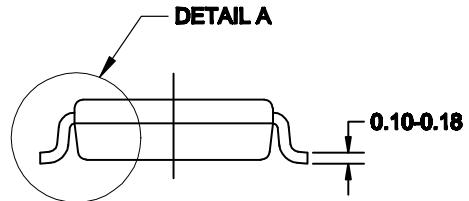
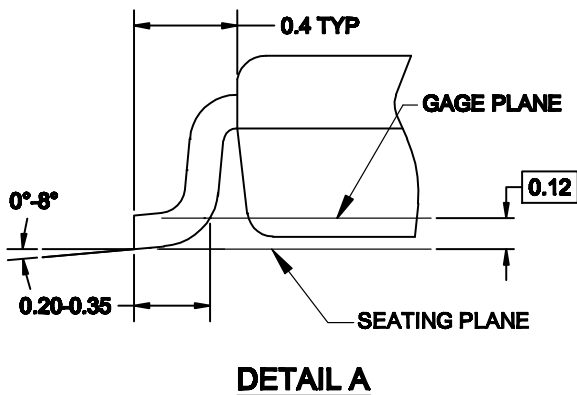
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- B. DIMENSIONS ARE IN MILLIMETERS.
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