

Features

- High speed
 - $t_{AA} = 17 \text{ ns}$
- Low active power
 - 1073 mW (max.)
- Low CMOS standby power
 - 2.75 mW (max.)
- 2.0 V data retention (400 μW at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features

Functional Description

The CY7C1049BN is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{\text{CE}}$), an active LOW Output Enable ($\overline{\text{OE}}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

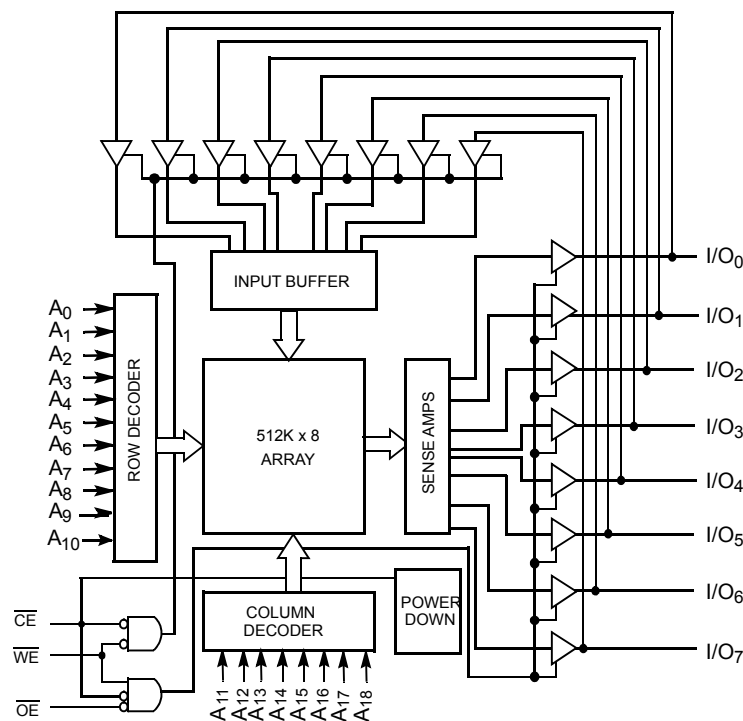
Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1049BN is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

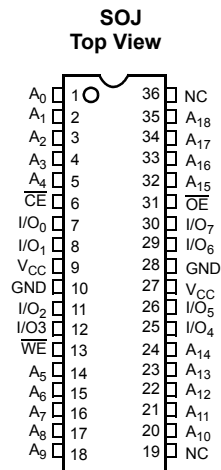


Contents

Pinouts	3	Ordering Code Definitions	11
Selection Guide	3	Package Diagram	12
Maximum Ratings	4	Acronyms	13
Operating Range	4	Document Conventions	13
Electrical Characteristics	4	Units of Measure	13
Capacitance	5	Document History Page	14
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	15
Data Retention Characteristics	5	Worldwide Sales and Design Support	15
Data Retention Waveform	5	Products	15
Switching Characteristics	6	PSoC® Solutions	15
Switching Waveforms	7	Cypress Developer Community	15
Truth Table	10	Technical Support	15
Ordering Information	11		

Pinouts

Figure 1. 36-pin SOJ pinout (Top View)



Selection Guide

Description	CY7C1049BNL-17
Maximum Access Time (ns)	17
Maximum Operating Current (mA)	195
Maximum CMOS Standby Current (mA)	0.5

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage on V_{CC} to Relative GND [1]	-0.5 V to +7.0 V
DC Voltage Applied to Outputs in High Z State [1]	-0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage [1]	-0.5 V to $V_{CC} + 0.5$ V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001 V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial L	0 °C to +70 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C1049B-17		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0$ mA	2.4	–	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0$ mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage [1]		-0.3	0.3	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	μ A
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	μ A
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $f = f_{MAX} = 1/t_{RC}$	–	195	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	40	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$, Commercial	–	0.5	mA

Note

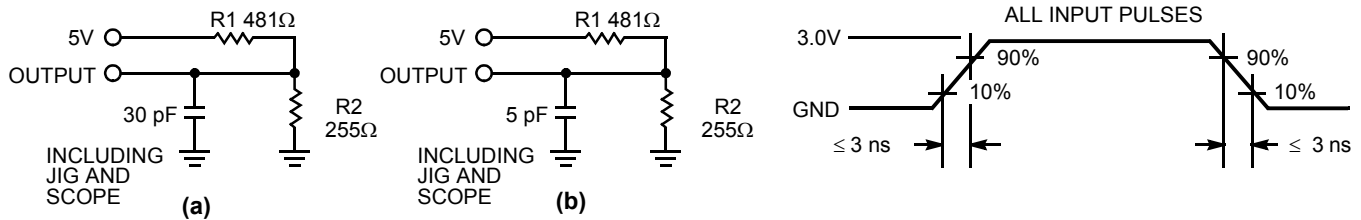
1. Minimum voltage is -2.0V for pulse durations of less than 20 ns.

Capacitance

Parameter ^[2]	Description	Test Conditions	Max.	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	8	pF
C _{OUT}	I/O capacitance		8	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT ○ — 167Ω — 1.73V

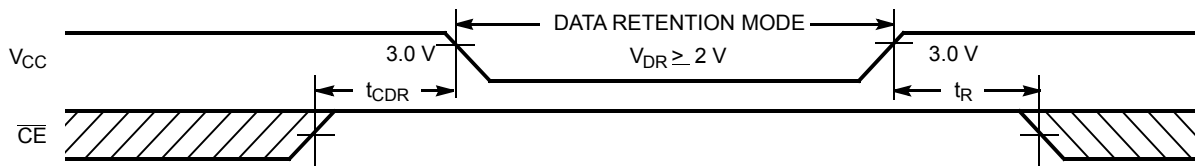
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions ^[3]		Min	Max	Unit
V _{DR}	V _{CC} for Data Retention			2.0	—	V
I _{CCDR}	Data Retention Current	Commercial	L	—	200	μA
t _{CDR} ^[2]	Chip Deselect to Data Retention Time	V _{CC} = V _{DR} = 3.0 V, CĒ ≥ V _{CC} - 0.3 V,		0	—	ns
t _R ^[4]	Operation Recovery Time	V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V		t _{RC}	—	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- 2. Tested initially and after any design or process changes that may affect these parameters.
- 3. No input may exceed V_{CC} + 0.5 V.
- 4. t_r ≤ 3 ns for the -12 and -15 speeds. t_r ≤ 5 ns for the -20 and slower speeds.

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description	CY7C1049BNL-17		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC} (typical) to the First Access ^[6]	1	–	ms
t_{RC}	Read Cycle Time	17	–	ns
t_{AA}	Address to Data Valid	–	17	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	\overline{CE} LOW to Data Valid	–	17	ns
t_{DOE}	\overline{OE} LOW to Data Valid	–	8	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[7]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]	–	7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[7]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]	–	7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0	–	ns
t_{PD}	\overline{CE} HIGH to Power-Down	–	17	ns
Write Cycle ^[9, 10]				
t_{WC}	Write Cycle Time	17	–	ns
t_{SCE}	\overline{CE} LOW to Write End	12	–	ns
t_{AW}	Address Set-Up to Write End	12	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-Up to Write Start	0	–	ns
t_{PWE}	\overline{WE} Pulse Width	12	–	ns
t_{SD}	Data Set-Up to Write End	8	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]	–	8	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 [11, 12]

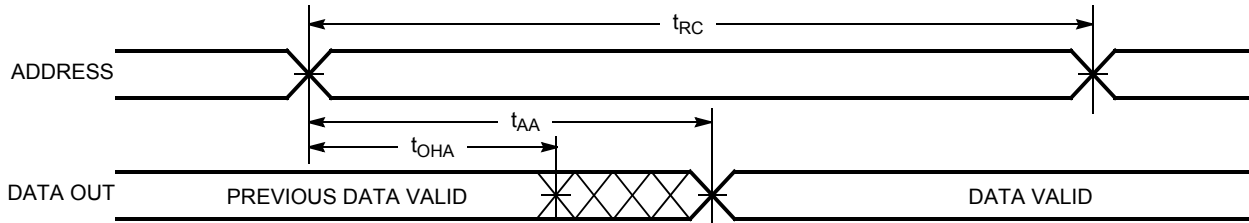
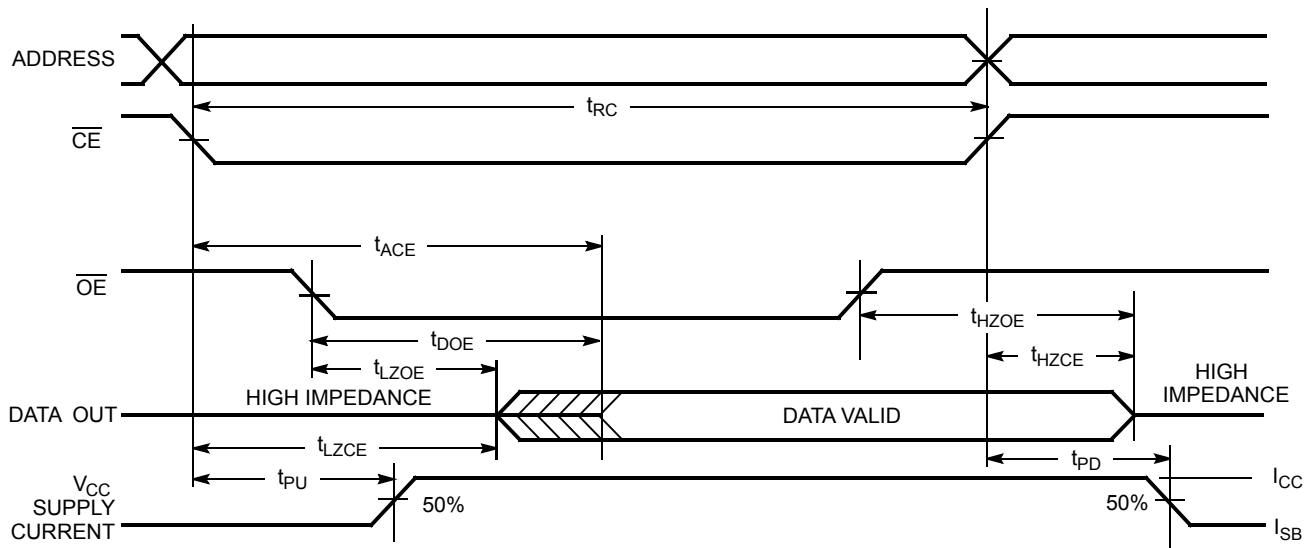


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]



Notes

11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.

12. \overline{WE} is HIGH for read cycle.

13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (\overline{CE} Controlled) [14, 15]

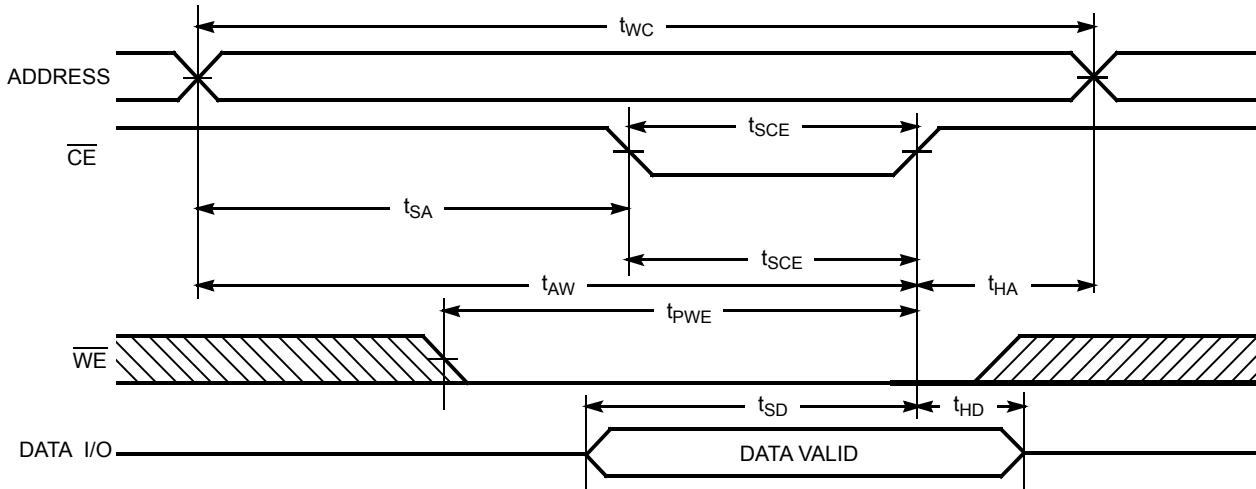
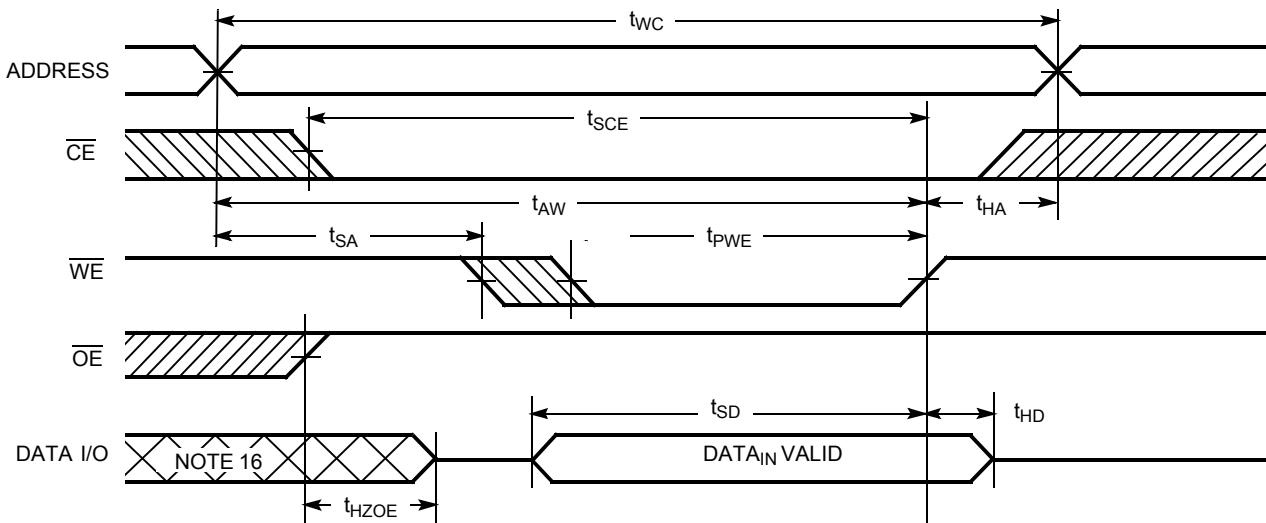
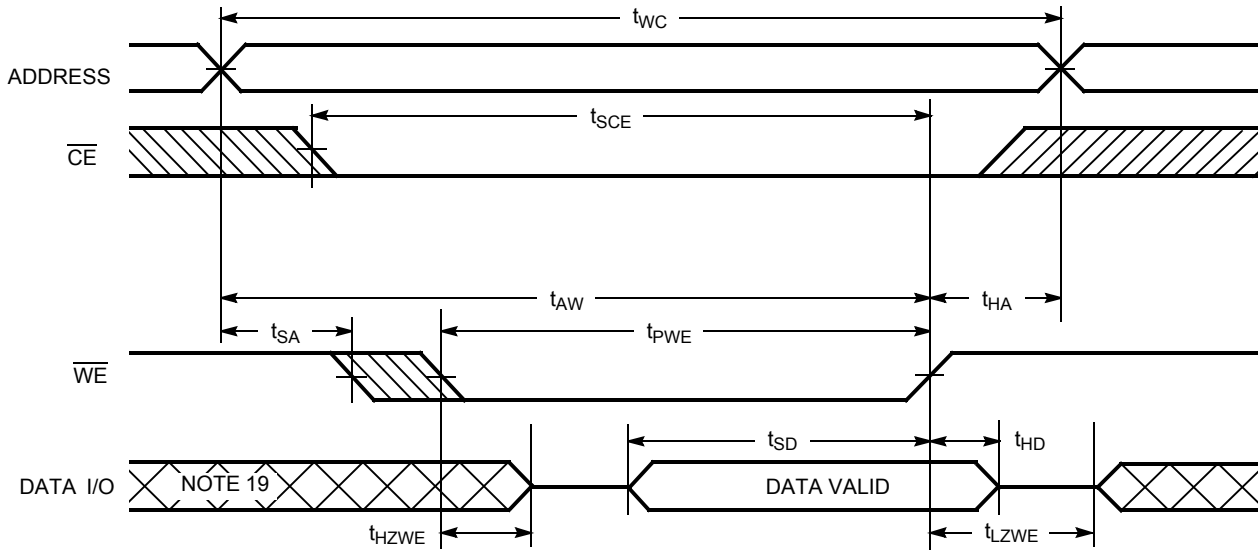


Figure 7. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH during Write) [14, 15]



Notes

- 14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 15. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)
Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [17, 18]

Notes

17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

18. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

19. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
\overline{OE}	Output Enable
SRAM	Static Random Access Memory
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1049BN, 512 K × 8 Static RAM Document Number: 001-76449				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3539227	TAVA	03/01/2012	New data sheet.
*A	4371513	VINI	05/06/2014	Updated Switching Waveforms : Added Note 18 and referred the same note in Figure 8 . Updated to new template. Completing Sunset Review.
*B	4573121	VINI	11/18/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end.
*C	4765735	VINI	05/14/2015	Updated Package Diagram : spec 51-85090 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*D	6012105	AESATP12	01/03/2018	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.