Low Power, 4 MHz GBW, Rail-to-Rail Input-Output Operational Amplifier in SOT-23 Package

Check for Samples: LM7301

FEATURES

- **At V_S = 5V (Typ Unless Otherwise Noted)**
- **Tiny 5-Pin SOT-23 Package Saves Space**
- **Greater than Rail-to-Rail Input CMVR −0.25V to 5.25V**
- **Rail-to-Rail Output Swing 0.07V to 4.93V**
- **Wide Gain-Bandwidth 4 MHz**
- **Low Supply Current 0.60 mA**
- **Wide Supply Range 1.8V to 32V**
- **High PSRR 104 dB**
- **High CMRR 93 dB**
- **Excellent Gain 97 dB**

APPLICATIONS

- **Portable Instrumentation**
- **Signal Conditioning Amplifiers/ADC Buffers**
- **Active Filters**
- **Modems**
- **PCMCIA Cards**

DESCRIPTION

The LM7301 provides high performance in a wide range of applications. The LM7301 offers greater than rail-to-rail input range, full rail-to-rail output swing, large capacitive load driving ability and low distortion.

With only 0.6 mA supply current, the 4 MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM7301 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies of 1.8V–32V, the LM7301 is excellent for a very wide range of applications in low power systems.

Placing the amplifier right at the signal source reduces board size and simplifies signal routing. The LM7301 fits easily on low profile PCMCIA cards.

Connection Diagrams

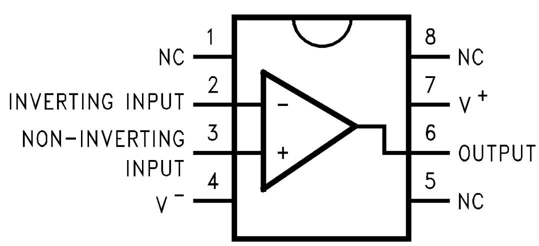

Figure 1. 8-Pin SOIC (Top View)
See Package Number D

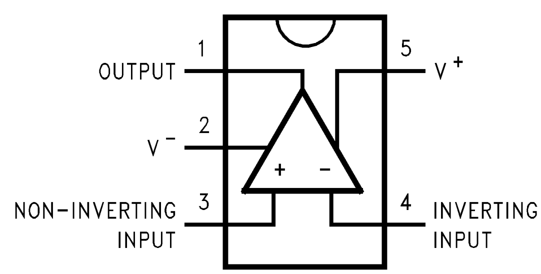

Figure 2. 5-Pin SOT-23 (Top View)
See Package Number DBV

Gain and Phase

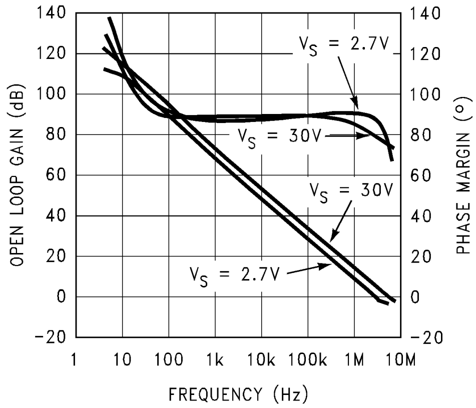

Figure 3.

Gain and Phase, 2.7V Supply

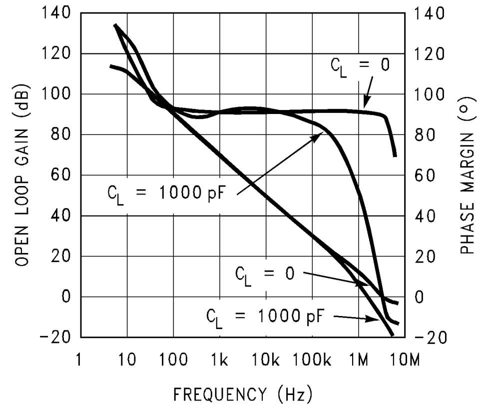

Figure 4.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

		Value	Unit
ESD Tolerance(3)	Human Body Model	2500	V
Differential Input Voltage		15	V
Voltage at Input/Output Pin		$(V^+) + 0.3V, (V^-) -0.3$	V
Supply Voltage $(V^+ - V^-)$		35	V
Current at Input Pin		±10	mA
Current at Output Pin(4)		±20	mA
Current at Power Supply Pin		25	mA
Soldering Information: http://www.ti.com/lit/an/snoa549c/snoa549c.pdf			
Storage Temperature Range		−65°C to +150	°C
Junction Temperature(5)		150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings(1)

		Value	Unit
Supply Voltage		$1.8 \le V_S \le 32$	V
Operating Temperature Range(2)		−40 to +85	°C
Package Thermal Resistance (θ_{JA})(2)	5-Pin SOT-23	325	°C/W
	8-Pin SOIC	165	°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

5.0V DC Electrical Characteristics[1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LM7301		Units
			Typ [2]	Limit [3]	
V_{OS}	Input Offset Voltage		0.03	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		μV/°C
I_B	Input Bias Current	V_{CM} = 0V	90	200 **250**	nA max
		V_{CM} = 5V	−40	−75 **−85**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	0.7	70 **80**	nA max
		V_{CM} = 5V	0.7	55 **65**	
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 5V	39		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	88	70 **67**	dB min
		0V ≤ V_{CM} ≤ 3.5V	93		
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 30V	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	5.1 −0.1		V V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ V_O = 4.0V_{PP}	71	14 **10**	V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.12 **0.15**	V max
			4.93	4.88 **4.85**	V min
		R_L = 2 kΩ	0.14	0.20 **0.22**	V max
			4.87	4.80 **4.78**	V min
I_{SC}	Output Short Circuit Current	Sourcing	11.0	8.0 **5.5**	mA min
		Sinking	9.5	6.0 **5.0**	mA min
I_S	Supply Current		0.60	1.10 **1.24**	mA max

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) All limits are guaranteed by testing or statistical analysis.

AC Electrical Characteristics(1)

T_A = 25°C, V^+ = 2.2V to 30V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1MΩ to $V^+/2$

Symbol	Parameter	Conditions	Typ (2)	Units
SR	Slew Rate	±4V Step @ V_S ±6V	1.25	V/µs
GBW	Gain-Bandwidth Product	f = 100 kHz, R_L = 10 kΩ	4	MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz	36	nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz	0.24	pA/√Hz
T.H.D.	Total Harmonic Distortion	f = 10 kHz	0.006	%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

2.2V DC Electrical Characteristics(1)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.2V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LM7301 Typ (2)	LM7301 Limit (3)	Units
V_{OS}	Input Offset Voltage		0.04	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	89	200 **250**	nA max
		V_{CM} = 2.2V	−35	−75 **−85**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	0.8	70 **80**	nA max
		V_{CM} = 2.2V	0.4	55 **65**	
R_{IN}	Input Resistance	0V ≤ V_{CM} ≤ 2.2V	18		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 2.2V	82	60 **56**	dB min
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 30V	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	2.3 −0.1		V V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ V_O = 1.6V_{PP}	46	6.5 **5.4**	V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.05	0.08 **0.10**	V max
			2.15	2.10 **2.00**	V min
		R_L = 2 kΩ	0.09	0.13 **0.14**	V max
			2.10	2.07 **2.00**	V min

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) All limits are guaranteed by testing or statistical analysis.

2.2V DC Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.2V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LM7301 Typ (2)	LM7301 Limit (3)	Units
I_{SC}	Output Short Circuit Current	Sourcing	10.9	8.0 **5.5**	mA min
		Sinking	7.7	6.0 **5.0**	mA min
I_S	Supply Current		0.57	0.97 **1.24**	mA max

30V DC Electrical Characteristics(1)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 30V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LM7301 Typ (2)	LM7301 Limit (3)	Units
V_{OS}	Input Offset Voltage		0.04	6 8	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		μV/°C
I_B	Input Bias Current	V_{CM} = 0V	103	300 **500**	nA max
		V_{CM} = 30V	−50	−100 **−200**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	1.2	90 **190**	nA max
		V_{CM} = 30V	0.5	65 **135**	nA max
R_{IN}	Input Resistance	0V ≤ V_{CM} ≤ 30V	200		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 30V	104	80 **78**	dB min
		0V ≤ V_{CM} ≤ 27V	115	90 **88**	
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 30V	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 80 dB	30.1 −0.1		V V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ V_O = 28V_{PP}	105	30 **20**	V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.16	0.275 **0.375**	V max
			29.8	29.75 **28.65**	V min
I_{SC}	Output Short Circuit Current	Sourcing (4)	11.7	8.8 **6.5**	mA min
		Sinking (4)	11.5	8.2 **6.0**	mA min

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) All limits are guaranteed by testing or statistical analysis.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

30V DC Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 30V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LM7301 Typ (2)	LM7301 Limit (3)	Units
I_S	Supply Current		0.72	**1.35** 1.30	mA max

Typical Performance Characteristics

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

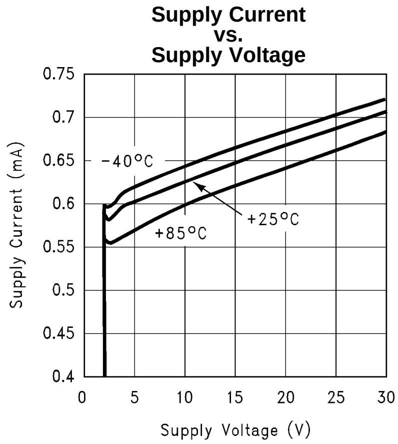

Figure 5.

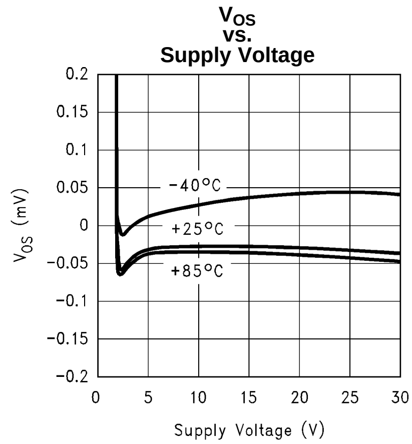

Figure 6.

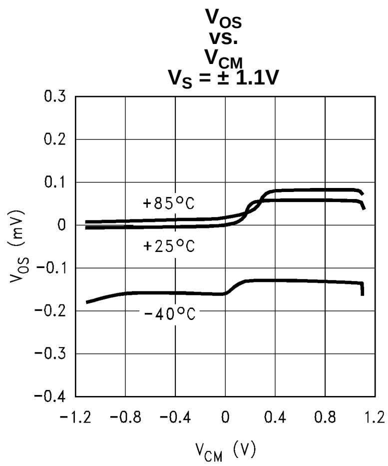

Figure 7.

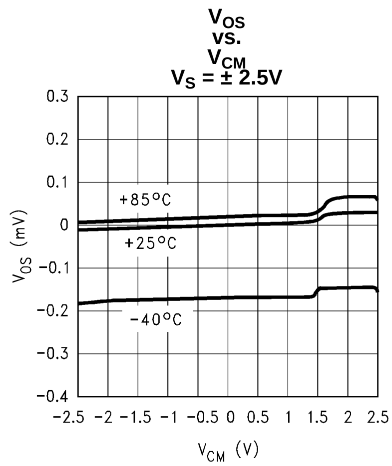

Figure 8.

Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

V_{OS} vs. V_{CM} V_S = ± 15V

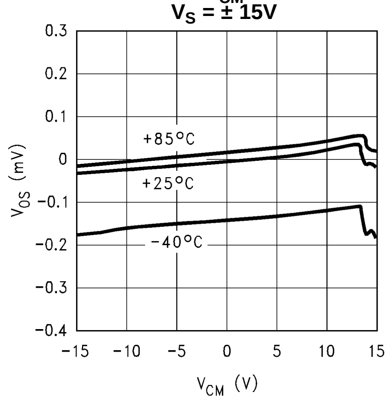

Figure 9.

Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 1.1V

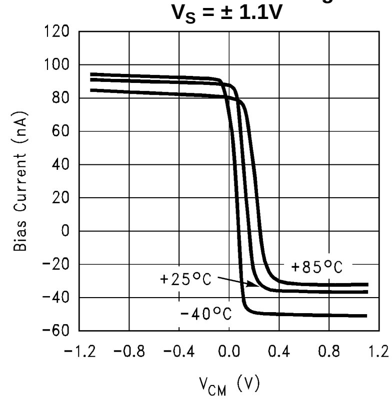

Figure 10.

Non-Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 1.1V

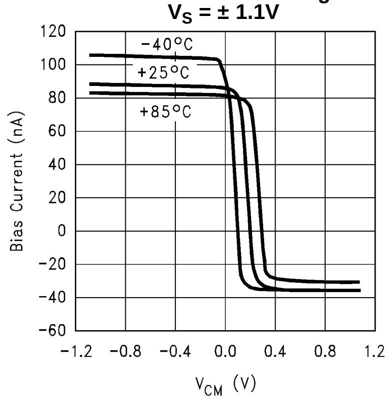

Figure 11.

Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 2.5V

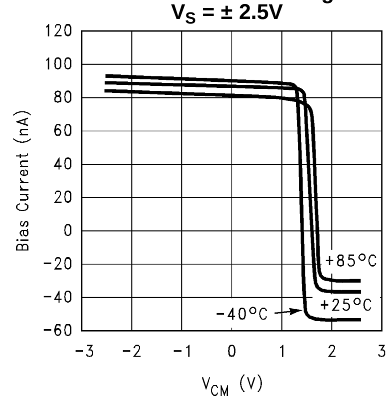

Figure 12.

Non-Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 2.5V

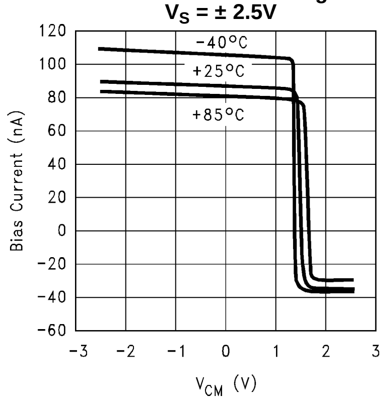

Figure 13.

Non-Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 15V

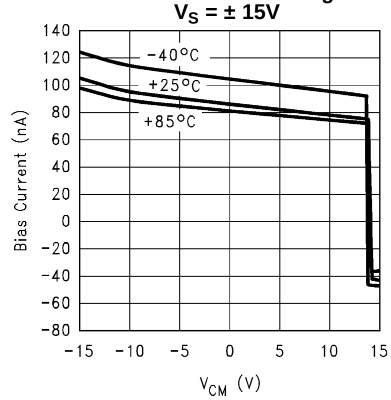

Figure 14.

Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

Inverting Input Bias Current vs. Common Mode Voltage V_S = ± 15V

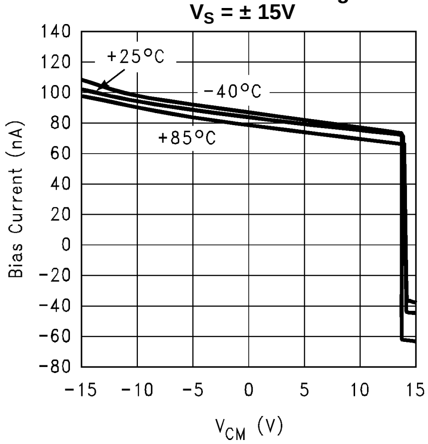

Figure 15.

V_O vs. I_O V_S = ± 1.1V

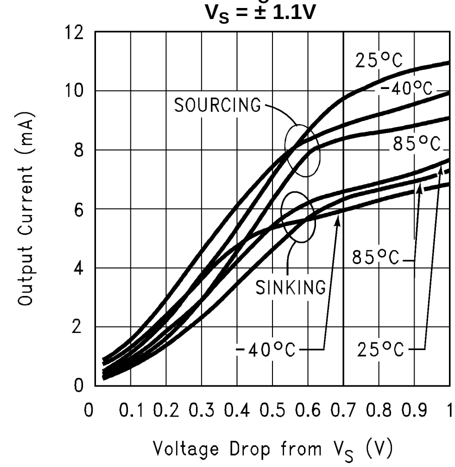

Figure 16.

V_O vs. I_O V_S = ± 2.5V

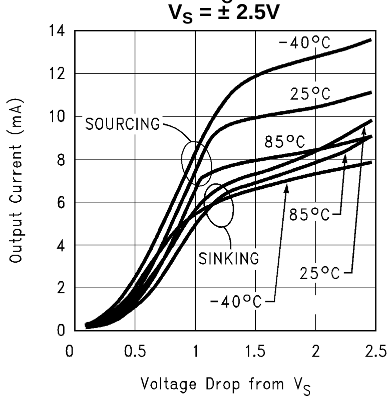

Figure 17.

Short Circuit Current vs. Supply Voltage

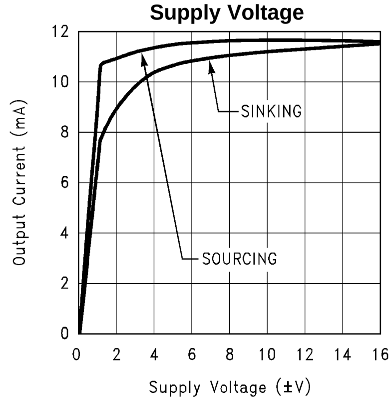

Figure 18.

Voltage Noise vs. Frequency

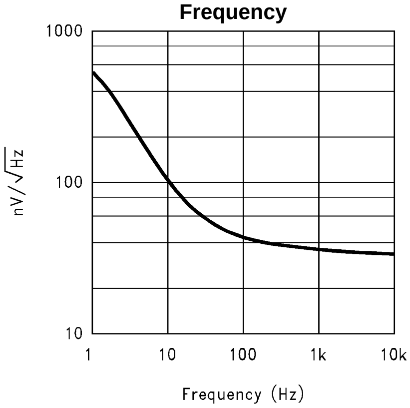

Figure 19.

Current Noise vs. Frequency

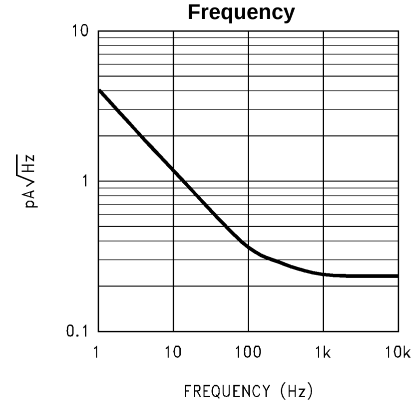

Figure 20.

Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

Gain and Phase

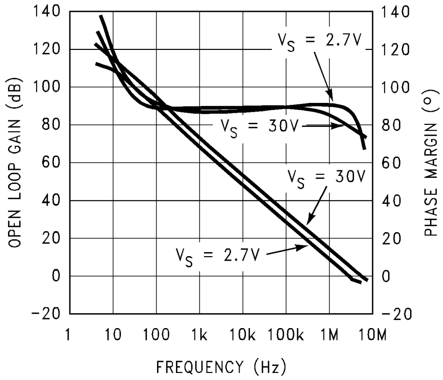

Figure 21.

Gain and Phase, 2.7V Supply

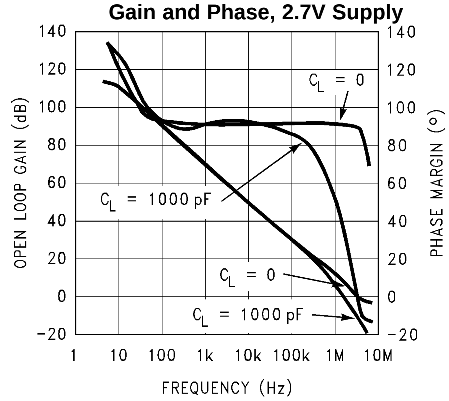

Figure 22.

APPLICATIONS INFORMATION

GENERAL INFORMATION

Low supply current, wide bandwidth, input common mode voltage range that includes both rails, "rail-to-rail" output, good capacitive load driving ability, wide supply voltage (1.8V to 32V) and low distortion all make the LM7301 ideal for many diverse applications.

The high common-mode rejection ratio and full rail-to-rail input range provides precision performance when operated in non-inverting applications where the common-mode error is added directly to the other system errors.

CAPACITIVE LOAD DRIVING

The LM7301 has the ability to drive large capacitive loads. For example, 1000 pF only reduces the phase margin to about 25 degrees.

TRANSIENT RESPONSE

The LM7301 offers a very clean, well-behaved transient response. Figure 23, Figure 24, Figure 25, Figure 26, Figure 27, Figure 28 show the response when operated at gains of +1 and −1 when handling both small and large signals. The large phase margin, typically 70 to 80 degrees, assures clean and symmetrical response. In the large signal scope photos, Figure 23 and Figure 26, the input signal is set to 4.8V. Note that the output goes to within 100 mV of the supplies cleanly and without overshoot. In the small signal samples, the response is clean, with only slight overshoot when used as a follower. Figure 25 and Figure 28 are the circuits used to make these photos.

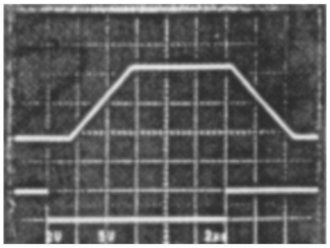

Figure 23.

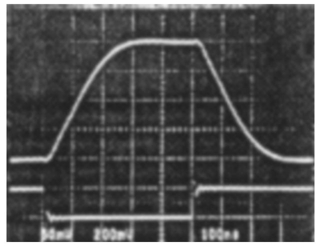

Figure 24.

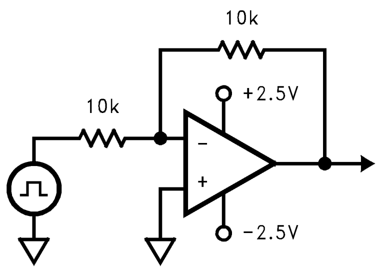

Figure 25.

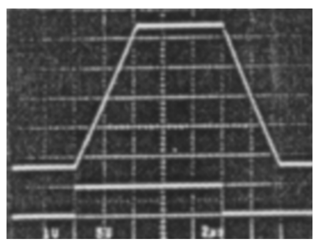

Figure 26.

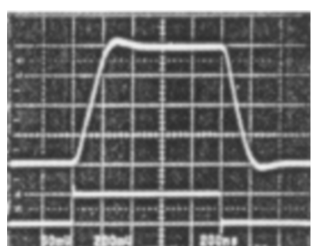

Figure 27.

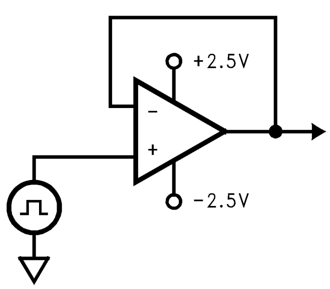

Figure 28.

STABILITY CONSIDERATIONS

Rail-to-rail output amplifiers like the LM7301 use the collector of the drive transistor(s) at the output pin, as shown in Figure 29. This allows the load to be driven as close as possible towards either supply rail.

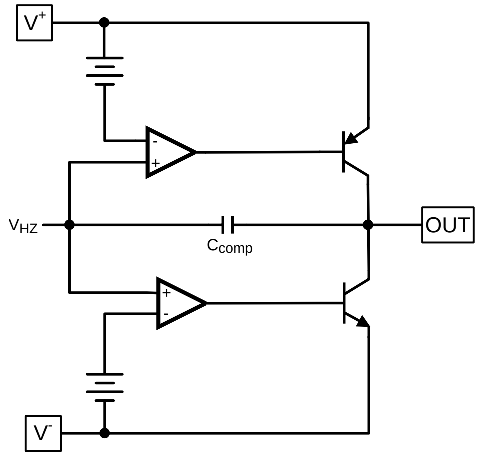

Figure 29. Simplified Output Stage Block Diagram

While this architecture maximizes the load voltage swing range, it increases the dependence of loop gain and subsequently stability, on load impedance and DC load current, compared to a non-rail-to-rail architecture. Thus, with this type of output stage, it is even more crucial to ensure stability by meticulous bench verification under all load conditions, and to apply the necessary compensation or circuit modifications to overcome any instability, if necessary. Any such bench verification should also include temperature, supply voltage, input common mode and output bias point variations as well as capacitive loading.

For example, one set of conditions for which stability of the LM7301 amplifier may be compromised is when the DC output load is larger than +/-0.5 mA, with input and output biased to mid-rail. Under such conditions, it may be possible to observe open-loop gain response peaking at a high frequency (e.g. 200 MHz), which is beyond the expected frequency range of the LM7301 (4 MHz GBW). Without taking any precautions against gain peaking, it is possible to see increased settling time or even oscillations, especially with low closed loop gain and / or light AC loading. It is possible to reduce or eliminate this gain peaking by using external compensation components. One possible scheme that can be applied to reduce or eliminate this gain peaking is shown in Figure 30.

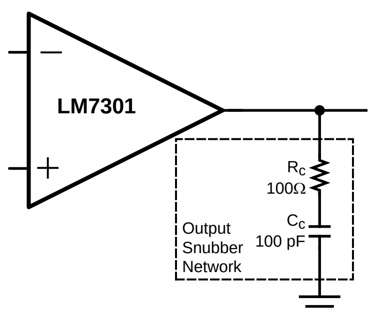

Figure 30. Non-dissipating Snubber Network to Reduce Gain Peaking

The non-dissipating snubber, consisting of R_c and C_c, acts as AC load to reduce high frequency gain peaking with no DC loading so that total power dissipation is not increased. The increased AC load effectively reduces loop gain at higher frequencies thereby reducing gain peaking due to the possible causes stated above. For the particular set of R_c and C_c values shown in Figure 30, loop gain peaking is reduced by about 25dB under worst case peaking conditions (I_source= 2mA DC @ around 180MHz) thus confining loop gain below 0dB and eliminating any possible instability. For best results, it may be necessary to “tune” the values of R_c and C_c in a particular application to take into account other subtleties and tolerances.

POWER DISSIPATION

Although the LM7301 has internal output current limiting, shorting the output to ground when operating on a +30V power supply will cause the op amp to dissipate about 350 mW. This is a worst-case example. In the 8-pin SOIC package, this will cause a temperature rise of 58°C. In the 5-pin SOT-23 package, the higher thermal resistance will cause a calculated rise of 113°C. This can raise the junction temperature to above the absolute maximum temperature of 150°C.

Operating from split supplies greatly reduces the power dissipated when the output is shorted. Operating on ±15V supplies can only cause a temperature rise of 29°C in the 8-pin SOIC and 57°C in the 5-pin SOT-23 package, assuming the short is to ground.

WIDE SUPPLY RANGE

The high power-supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) provide precision performance when operated on battery or other unregulated supplies. This advantage is further enhanced by the very wide supply range (2.2V–30V, guaranteed) offered by the LM7301. In situations where highly variable or unregulated supplies are present, the excellent PSRR and wide supply range of the LM7301 benefit the system designer with continued precision performance, even in such adverse supply conditions.

SPECIFIC ADVANTAGES OF 5-Pin SOT-23 (TinyPak)

The obvious advantage of the 5-pin SOT-23, TinyPak, is that it can save board space, a critical aspect of any portable or miniaturized system design. The need to decrease overall system size is inherent in any handheld, portable, or lightweight system application.

Furthermore, the low profile can help in height limited designs, such as consumer hand-held remote controls, sub-notebook computers, and PCMCIA cards.

An additional advantage of the tiny package is that it allows better system performance due to ease of package placement. Because the tiny package is so small, it can fit on the board right where the op amp needs to be placed for optimal performance, unconstrained by the usual space limitations. This optimal placement of the tiny package allows for many system enhancements, not easily achieved with the constraints of a larger package. For example, problems such as system noise due to undesired pickup of digital signals can be easily reduced or mitigated. This pick-up problem is often caused by long wires in the board layout going to or from an op amp. By placing the tiny package closer to the signal source and allowing the LM7301 output to drive the long wire, the signal becomes less sensitive to such pick-up. An overall reduction of system noise results.

Often times system designers try to save space by using dual or quad op amps in their board layouts. This causes a complicated board layout due to the requirement of routing several signals to and from the same place on the board. Using the tiny op amp eliminates this problem.

Additional space savings parts are available in tiny packages from Texas Instruments, including low power amplifiers, precision voltage references, and voltage regulators.

LOW DISTORTION, HIGH OUTPUT DRIVE CAPABILITY

The LM7301 offers superior low-distortion performance, with a total-harmonic-distortion-plus-noise of 0.06% at f = 10 kHz. The advantage offered by the LM7301 is its low distortion levels, even at high output current and low load resistance. Please refer to STABILITY CONSIDERATIONS for methods used to ensure stability under all load conditions.

Typical Applications

HANDHELD REMOTE CONTROLS

The LM7301 offers outstanding specifications for applications requiring good speed/power trade-off. In applications such as remote control operation, where high bandwidth and low power consumption are needed. The LM7301 performance can easily meet these requirements.

OPTICAL LINE ISOLATION FOR MODEMS

The combination of the low distortion and good load driving capabilities of the LM7301 make it an excellent choice for driving opto-coupler circuits to achieve line isolation for modems. This technique prevents telephone line noise from coupling onto the modem signal. Superior isolation is achieved by coupling the signal optically from the computer modem to the telephone lines; however, this also requires a low distortion at relatively high currents. Due to its low distortion at high output drive currents, the LM7301 fulfills this need, in this and in other telecom applications. Please refer to STABILITY CONSIDERATIONS for methods used to ensure stability under all load conditions.

REMOTE MICROPHONE IN PERSONAL COMPUTERS

Remote microphones in Personal Computers often utilize a microphone at the top of the monitor which must drive a long cable in a high noise environment. One method often used to reduce the nose is to lower the signal impedance, which reduces the noise pickup. In this configuration, the amplifier usually requires 30 db–40 db of gain, at bandwidths higher than most low-power CMOS parts can achieve. The LM7301 offers the tiny package, higher bandwidths, and greater output drive capability than other rail-to-rail input/output parts can provide for this application.

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7301IM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM73 01IM	Samples
LM7301IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM73 01IM	Samples
LM7301IM5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A04A	Samples
LM7301IM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A04A	Samples
LM7301IM5X	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A04A	Samples
LM7301IM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A04A	Samples
LM7301IMX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM73 01IM	Samples
LM7301IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM73 01IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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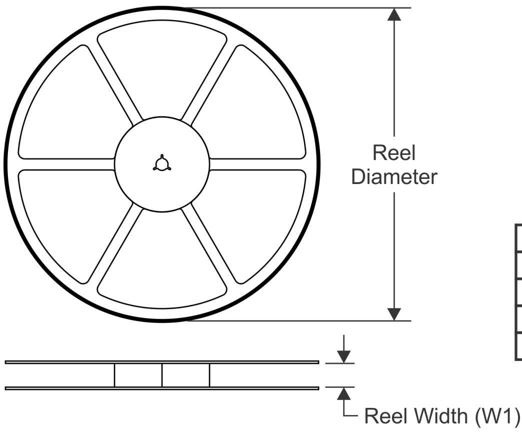
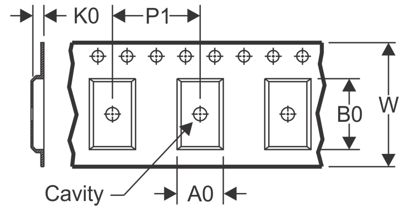
TAPE AND REEL INFORMATION

REEL DIMENSIONS

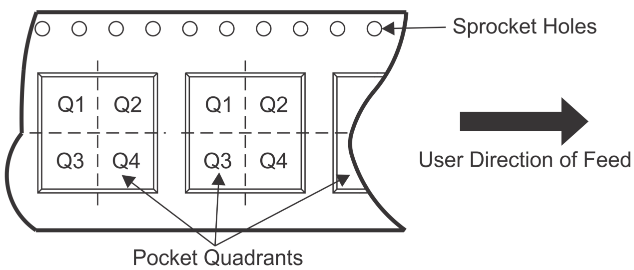


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

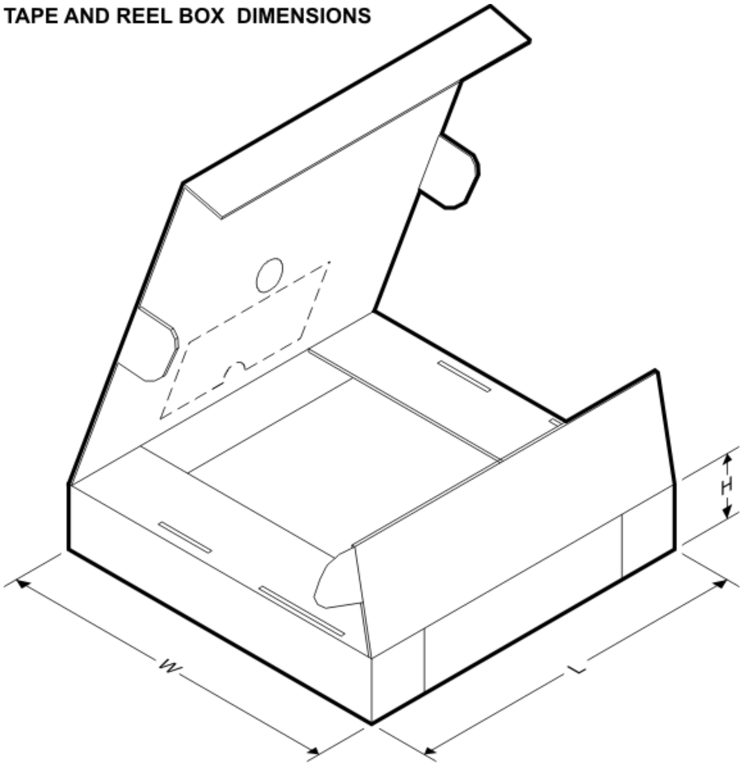
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7301IM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

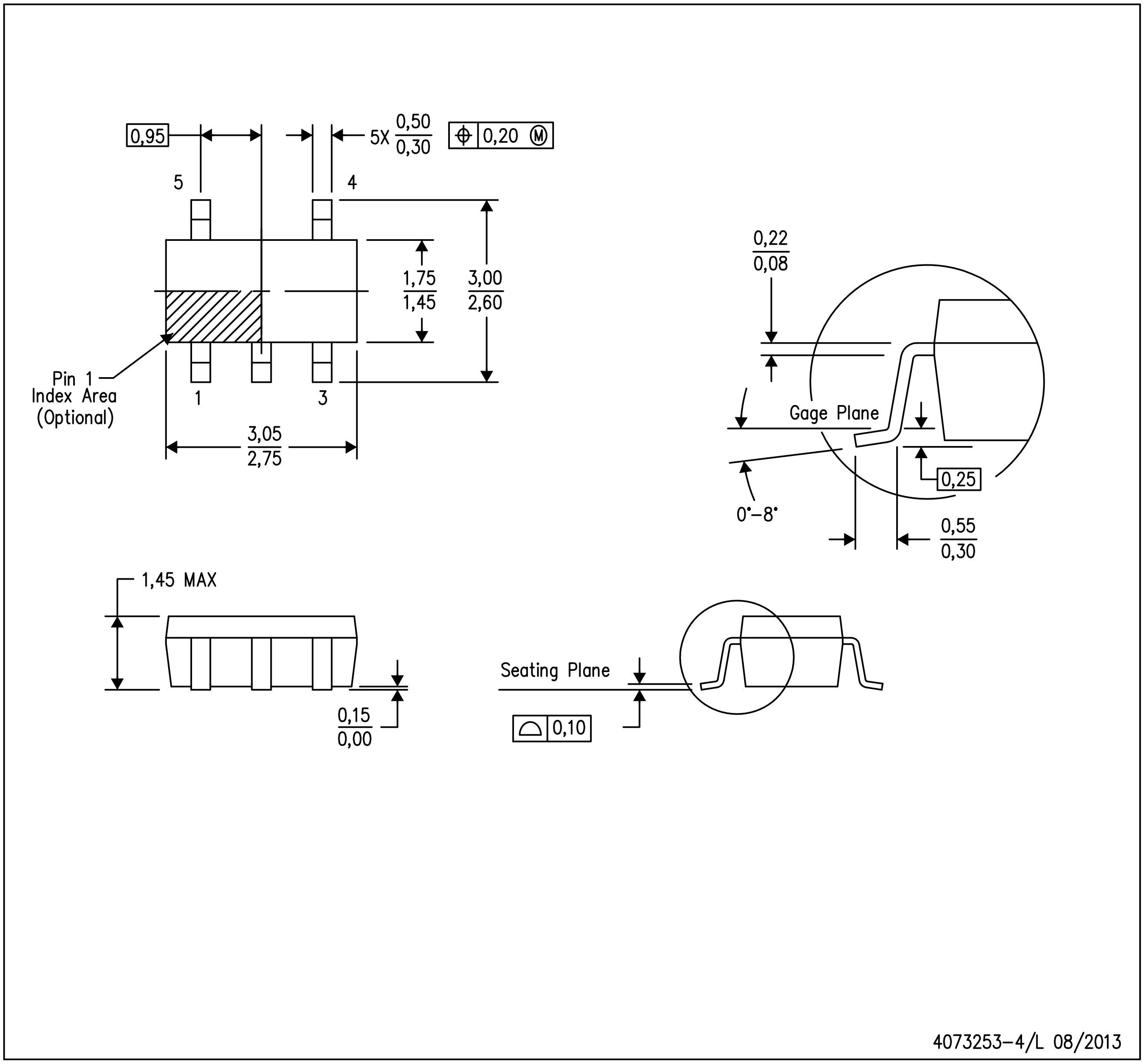
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

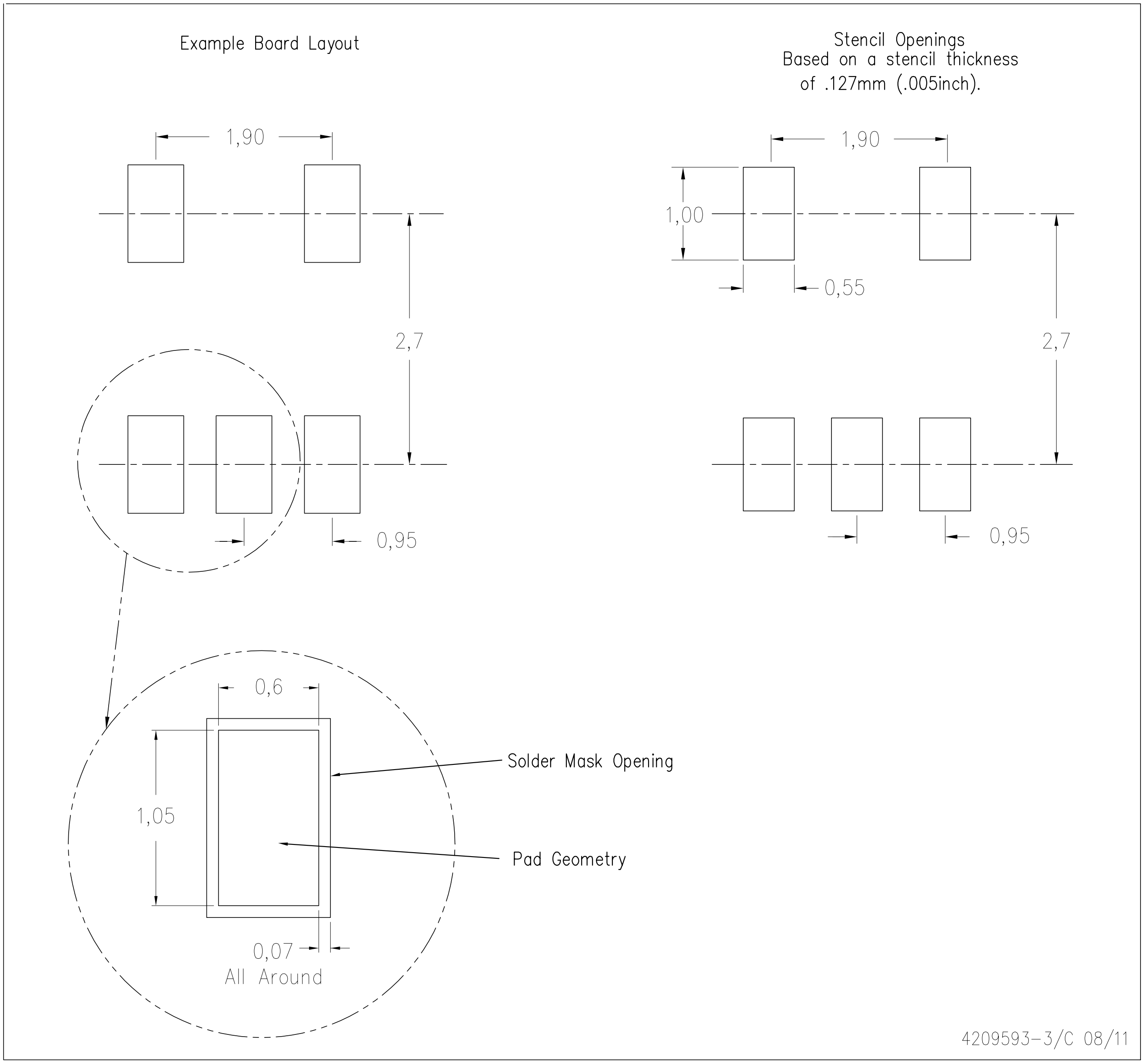
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7301IM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7301IM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7301IM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7301IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



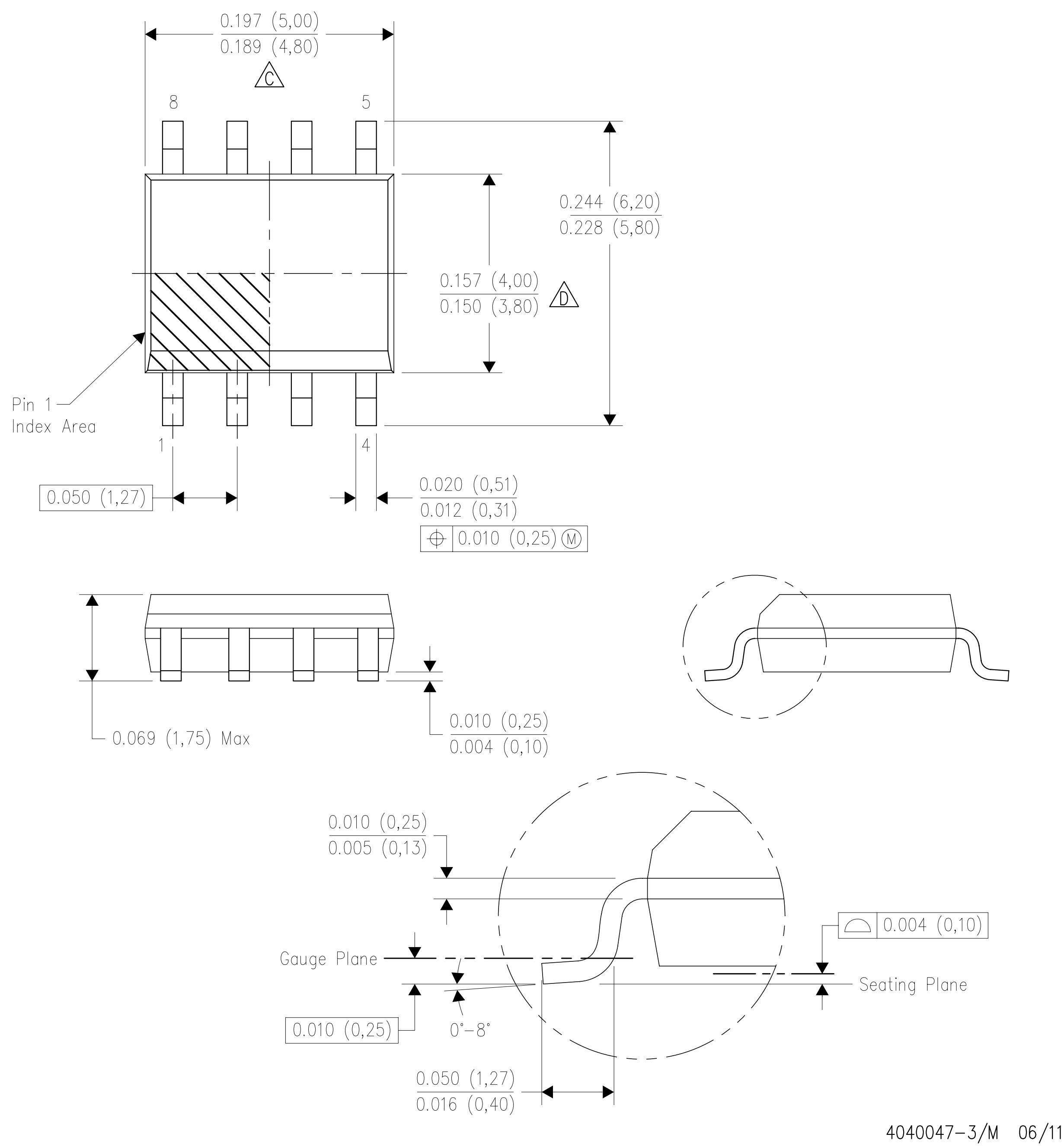
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

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