

Single, Dual, Quad Low-Voltage, Rail-to-Rail Operational Amplifiers

LMV321, NCV321, LMV358, LMV324

The LMV321, LMV321I, NCV321, LMV358/LMV358I and LMV324 are CMOS single, dual, and quad low voltage operational amplifiers with rail-to-rail output swing. These amplifiers are a cost-effective solution for applications where low power consumption and space saving packages are critical. Specification tables are provided for operation from power supply voltages at 2.7 V and 5 V. Rail-to-Rail operation provides improved signal-to-noise performance. Ultra low quiescent current makes this series of amplifiers ideal for portable, battery operated equipment. The common mode input range includes ground making the device useful for low-side current-shunt measurements. The ultra small packages allow for placement on the PCB in close proximity to the signal source thereby reducing noise pickup.

Features

- Operation from 2.7 V to 5.0 V Single-Sided Power Supply
- LMV321 Single Available in Ultra Small 5 Pin SC70 Package
- No Output Crossover Distortion
- Rail-to-Rail Output
- Low Quiescent Current: LMV358 Dual – 220 μ A, Max per Channel
- No Output Phase-Reversal from Overdriven Input
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

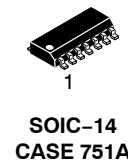
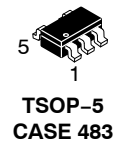
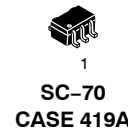
Typical Applications

- Notebook Computers and PDA's
- Portable Battery-Operated Instruments
- Active Filters



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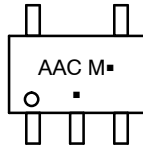
ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

LMV321, NCV321, LMV358, LMV324

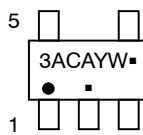
MARKING DIAGRAMS

SC-70



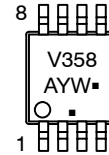
AAC = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

TSOP-5



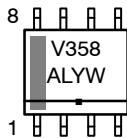
3AC = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

Micro8



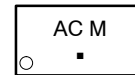
V358 = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

SOIC-8



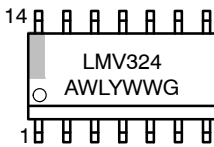
V358 = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

UDFN8



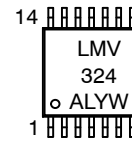
AC = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

SOIC-14



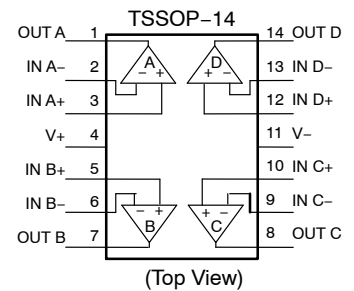
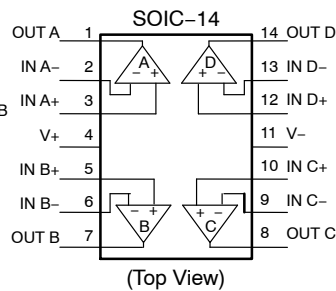
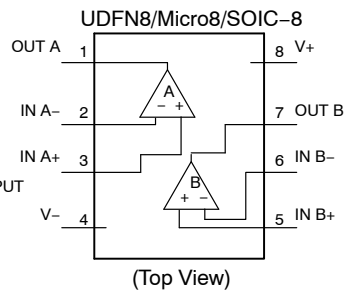
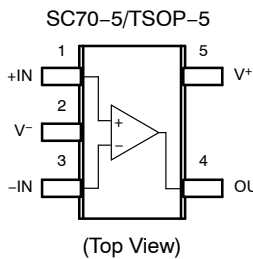
LMV324 = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

TSSOP-14



LMV324 = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

PIN CONNECTIONS



LMV321, NCV321, LMV358, LMV324

MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|------------------|--|--|---|
| V _S | Supply Voltage (Operating Range V _S = 2.7 V to 5.5 V) | 5.5 | V |
| V _{IDR} | Input Differential Voltage | ± Supply Voltage | V |
| V _{ICR} | Input Common Mode Voltage Range | -0.5 to (V+) + 0.5 | V |
| | Maximum Input Current | 10 | mA |
| t _{So} | Output Short Circuit (Note 1) | Continuous | |
| T _J | Maximum Junction Temperature | 150 | °C |
| T _A | Operating Ambient Temperature Range | LMV321, LMV358, LMV324 LMV321, LMV358I NCV321 (Note 2) | -40 to 85 -40 to 125 -40 to 125 °C °C °C |
| θ _{JA} | Thermal Resistance: | | °C/W |
| | SC-70 | 280 | |
| | Micro8 | 238 | |
| | TSOP-5 | 333 | |
| | UDFN8 (1.2 mm x 1.8 mm x 0.5 mm) | 350 | |
| | SOIC-8 | 212 | |
| | SOIC-14 | 156 | |
| | TSSOP-14 | 190 | |
| T _{stg} | Storage Temperature | -65 to 150 | °C |
| | Mounting Temperature (Infrared or Convection -20 sec) | 260 | °C |
| V _{ESD} | ESD Tolerance (Note 3) | | V |
| | LMV321, LMV321I, NCV321 Machine Model | 100 | |
| | Human Body Model | 1000 | |
| | LMV358/358I/324 Machine Model | 100 | |
| Human Body Mode | 2000 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Continuous short-circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V- will adversely affect reliability.
2. NCV prefix is qualified for automotive usage.
3. Human Body Model, applicable std. MIL-STD-883, Method 3015.7
Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)
Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

LMV321, NCV321, LMV358, LMV324

2.7 V DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{ V}$, $R_L = 1\text{ M}\Omega$, $V^- = 0\text{ V}$, $V_O = V^+/2$)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------|---|----------------|------------------|-------------------|------------------------------|
| Input Offset Voltage | V_{IO} | $T_A = T_{Low}$ to T_{High} (Note 4) | | 1.7 | 9 | mV |
| Input Offset Voltage Average Drift | ICV_{OS} | $T_A = T_{Low}$ to T_{High} (Note 4) | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $T_A = T_{Low}$ to T_{High} (Note 4) | | <1 | | nA |
| Input Offset Current | I_{IO} | $T_A = T_{Low}$ to T_{High} (Note 4) | | <1 | | nA |
| Common Mode Rejection Ratio | CMRR | $0\text{ V} \leq V_{CM} \leq 1.7\text{ V}$ | 50 | 63 | | dB |
| Power Supply Rejection Ratio | PSRR | $2.7\text{ V} \leq V^+ \leq 5\text{ V}$, $V_O = 1\text{ V}$ | 50 | 60 | | dB |
| Input Common-Mode Voltage Range | V_{CM} | For CMRR $\geq 50\text{ dB}$ | 0 to 1.7 | -0.2 to 1.9 | | V |
| Output Swing | V_{OH} | $R_L = 10\text{ k}\Omega$ to 1.35 V | $V_{CC} - 100$ | $V_{CC} - 10$ | | mV |
| | V_{OL} | $R_L = 10\text{ k}\Omega$ to 1.35 V (Note 5) | | 60 | 180 | mV |
| Supply Current LMV321, NCV321 LMV358/LMV358I (Both Amplifiers) LMV324 (4 Amplifiers) | I_{CC} | | | 80 140 260 | 185 340 680 | μA |

2.7 V AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{ V}$, $R_L = 1\text{ M}\Omega$, $V^- = 0\text{ V}$, $V_O = V^+/2$)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|------------------------------|------------|-----------------------|-----|-----|-----|------------------------------|
| Gain Bandwidth Product | GBWP | $C_L = 200\text{ pF}$ | | 1 | | MHz |
| Phase Margin | Θ_m | | | 60 | | $^\circ$ |
| Gain Margin | G_m | | | 10 | | dB |
| Input-Referred Voltage Noise | e_n | $f = 50\text{ kHz}$ | | 50 | | $\text{nV}/\sqrt{\text{Hz}}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. For LMV321, LMV358, LMV324: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
For LMV321I, LMV358I, NCV321: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.
5. Guaranteed by design and/or characterization.

LMV321, NCV321, LMV358, LMV324

5.0 V DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5.0\text{ V}$, $R_L = 1\text{ M}\Omega$, $V^- = 0\text{ V}$, $V_O = V^+/2$)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|------------------------------------|--------------|--|----------------------------------|---------------|-------------|------------------------------|
| Input Offset Voltage | V_{IO} | $T_A = T_{Low}$ to T_{High} (Note 6) | | 1.7 | 9 | mV |
| Input Offset Voltage Average Drift | $T_C V_{IO}$ | $T_A = T_{Low}$ to T_{High} (Note 6) | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current (Note 7) | I_B | $T_A = T_{Low}$ to T_{High} (Note 6) | | < 1 | | nA |
| Input Offset Current (Note 7) | I_{IO} | $T_A = T_{Low}$ to T_{High} (Note 6) | | < 1 | | nA |
| Common Mode Rejection Ratio | CMRR | $0\text{ V} \leq V_{CM} \leq 4\text{ V}$ | 50 | 65 | | dB |
| Power Supply Rejection Ratio | PSRR | $2.7\text{ V} \leq V^+ \leq 5\text{ V}$, $V_O = 1\text{ V}$, $V_{CM} = 1\text{ V}$ | 50 | 60 | | dB |
| Input Common-Mode Voltage Range | V_{CM} | For CMRR $\geq 50\text{ dB}$ | 0 to 4 | -0.2 to 4.2 | | V |
| Large Signal Voltage Gain (Note 7) | A_V | $R_L = 2\text{ k}\Omega$ | 15 | 100 | | V/mV |
| | | $T_A = T_{Low}$ to T_{High} (Note 6) | 10 | | | |
| Output Swing | V_{OH} | $R_L = 2\text{ k}\Omega$ to 2.5 V $T_A = T_{Low}$ to T_{High} (Note 6) | $V_{CC} - 300$ $V_{CC} - 400$ | $V_{CC} - 40$ | | mV |
| | V_{OL} | $R_L = 2\text{ k}\Omega$ to 2.5 V (Note 7) $T_A = T_{Low}$ to T_{High} (Note 6) | | 120 | 300 400 | mV |
| | V_{OH} | $R_L = 10\text{ k}\Omega$ to 2.5 V (Note 7) $T_A = T_{Low}$ to T_{High} (Note 6) | $V_{CC} - 100$ $V_{CC} - 200$ | | | mV |
| | V_{OL} | $R_L = 10\text{ k}\Omega$ to 2.5 V $T_A = T_{Low}$ to T_{High} (Note 6) | | 65 | 180 280 | mV |
| Output Short Circuit Current | I_O | Sourcing = $V_O = 0\text{ V}$ (Note 7) | 10 | 60 | | mA |
| | | Sinking = $V_O = 5\text{ V}$ (Note 7) | 10 | 160 | | |
| Supply Current | I_{CC} | LMV321 $T_A = T_{Low}$ to T_{High} (Note 6) | | 130 | 250 350 | μA |
| | | NCV321 $T_A = T_{Low}$ to T_{High} (Note 6) | | 130 | 250 350 | |
| | | LMV358/358I Both Amplifiers $T_A = T_{Low}$ to T_{High} (Note 6) | | 210 | 440 615 | |
| | | LMV324 All Four Amplifiers $T_A = T_{Low}$ to T_{High} (Note 6) | | 410 | 830 1160 | |

5.0 V AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5.0\text{ V}$, $R_L = 1\text{ M}\Omega$, $V^- = 0\text{ V}$, $V_O = V^+/2$)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|------------------------------|------------|-----------------------|-----|-----|-----|------------------------------|
| Slew Rate | S_R | | | 1 | | V/ μs |
| Gain Bandwidth Product | GBWP | $C_L = 200\text{ pF}$ | | 1 | | MHz |
| Phase Margin | θ_m | | | 60 | | $^\circ$ |
| Gain Margin | G_m | | | 10 | | dB |
| Input-Referred Voltage Noise | e_n | $f = 50\text{ kHz}$ | | 50 | | $\text{nV}/\sqrt{\text{Hz}}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. For LMV321, LMV358, LMV324: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
 For LMV321I, LMV358I, NCV321: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.
7. Guaranteed by design and/or characterization.

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

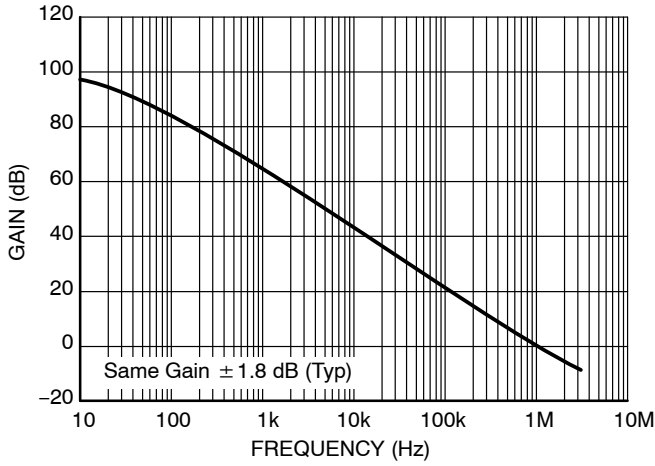


Figure 1. Open Loop Frequency Response
($R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$)

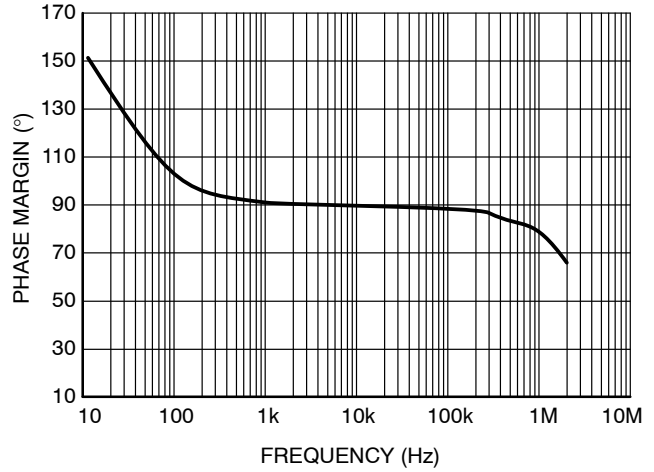


Figure 2. Open Loop Phase Margin
($R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$)

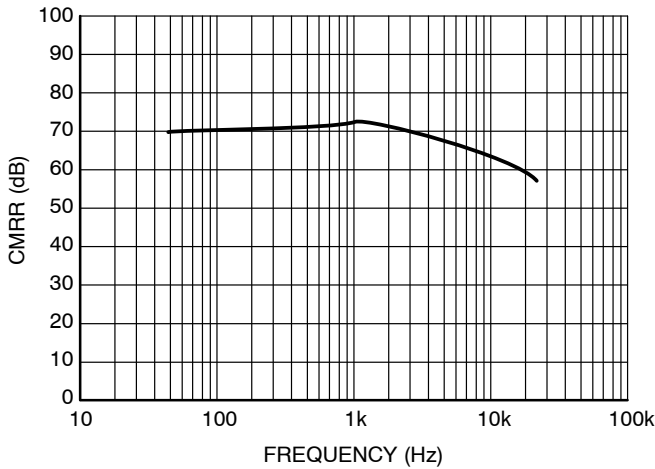


Figure 3. CMRR vs. Frequency
($R_L = 5\text{ k}\Omega$, $V_S = 5\text{ V}$)

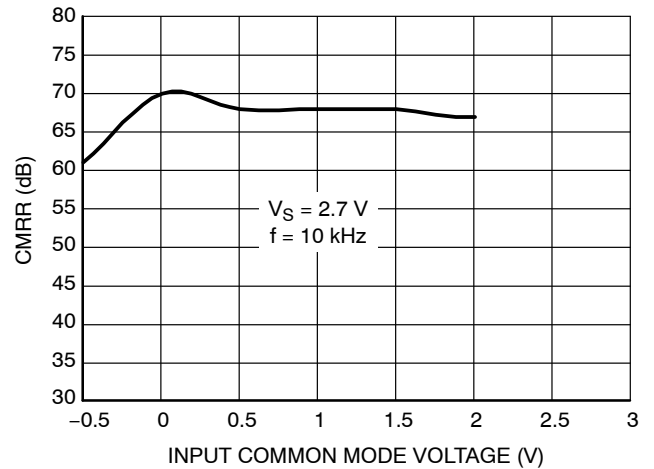


Figure 4. CMRR vs. Input Common Mode Voltage

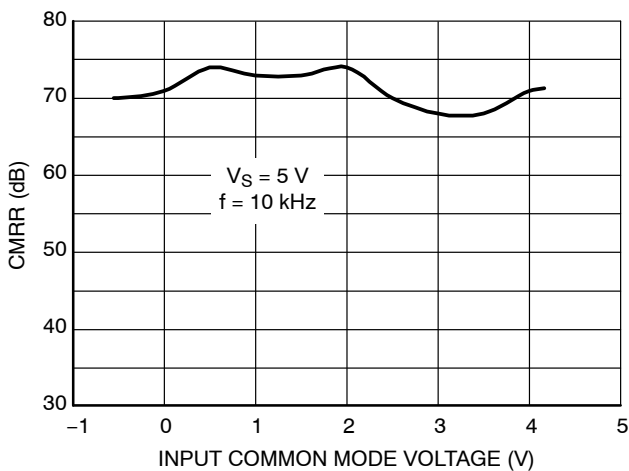


Figure 5. CMRR vs. Input Common Mode Voltage

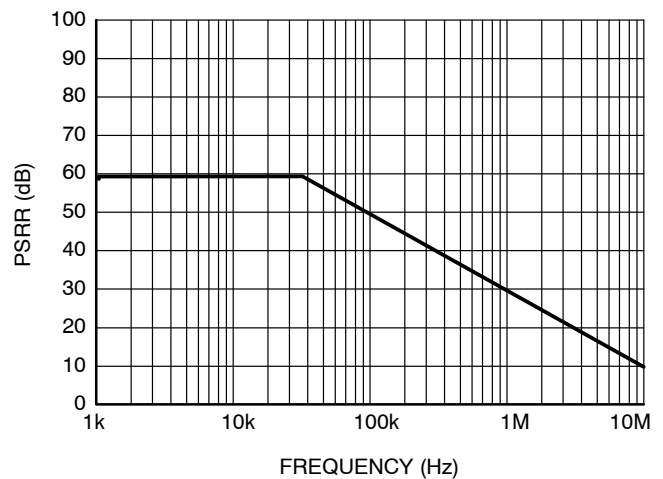


Figure 6. PSRR vs. Frequency
($R_L = 5\text{ k}\Omega$, $V_S = 2.7\text{ V}$, +PSRR)

LMV321, NCV321, LMV358, LMV324

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)



Figure 7. PSRR vs. Frequency
($R_L = 5\text{ k}\Omega$, $V_S = 2.7\text{ V}$, -PSRR)

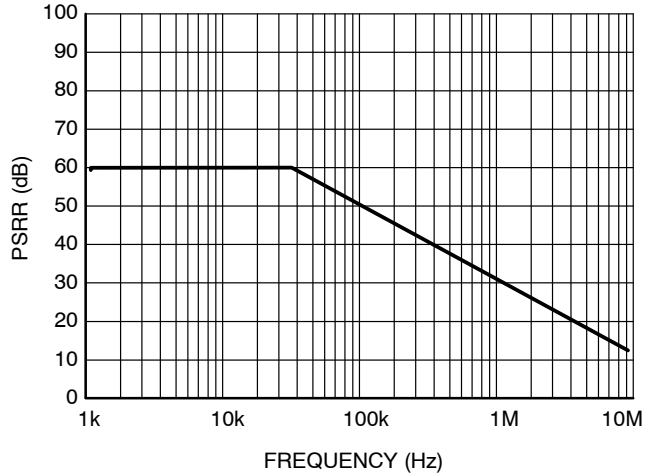


Figure 8. PSRR vs. Frequency
($R_L = 5\text{ k}\Omega$, $V_S = 5\text{ V}$, +PSRR)



Figure 9. PSRR vs. Frequency
($R_L = 5\text{ k}\Omega$, $V_S = 5\text{ V}$, -PSRR)

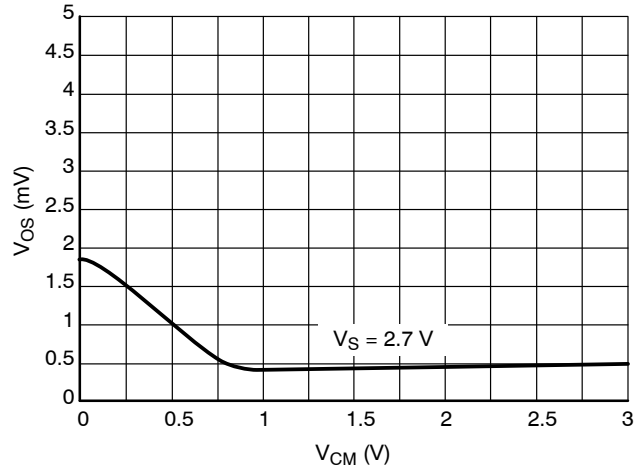


Figure 10. V_{OS} vs. CMR



Figure 11. V_{OS} vs. CMR

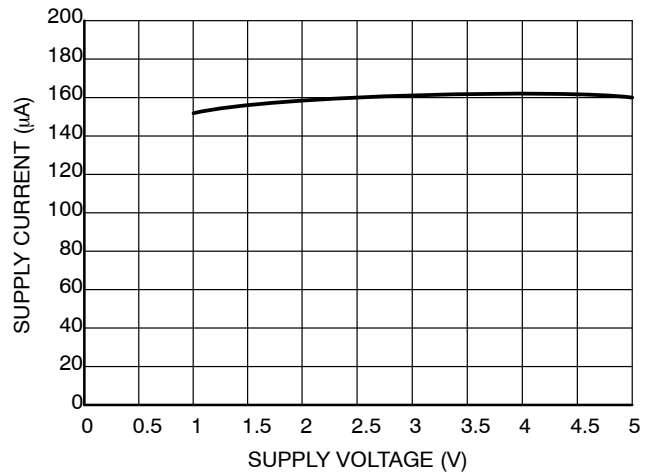


Figure 12. Supply Current vs. Supply Voltage

LMV321, NCV321, LMV358, LMV324

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)



Figure 13. THD+N vs Frequency

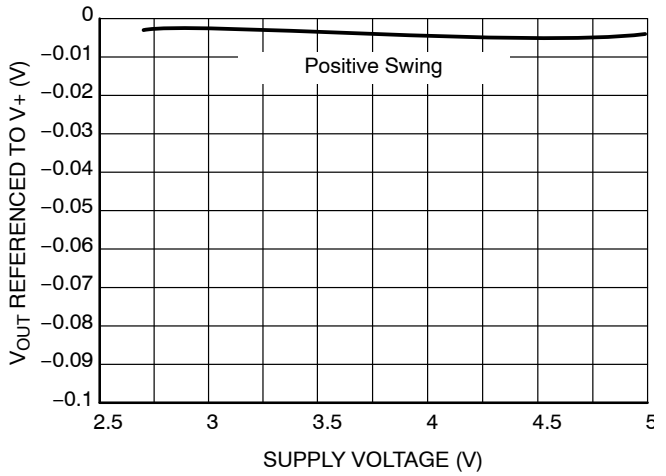


Figure 14. Output Voltage Swing vs Supply Voltage ($R_L = 10\text{ k}\Omega$)

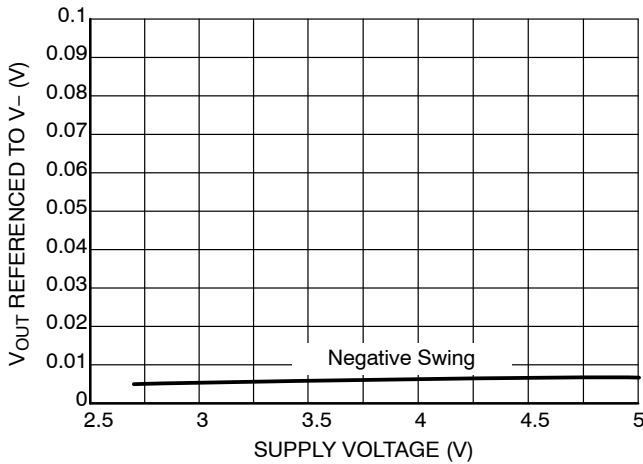


Figure 15. Output Voltage Swing vs Supply Voltage ($R_L = 10\text{ k}\Omega$)

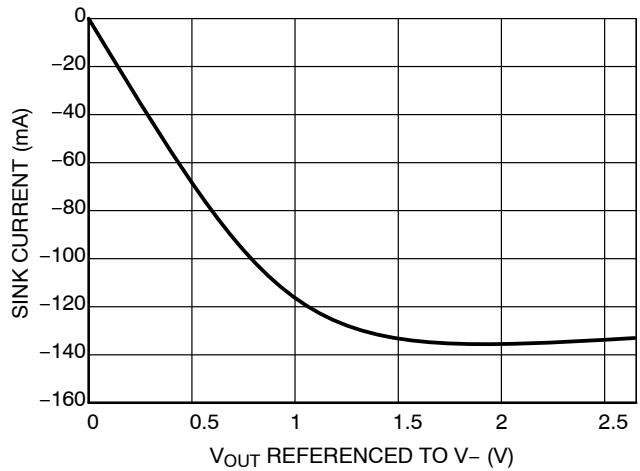


Figure 16. Sink Current vs. Output Voltage
 $V_S = 2.7\text{ V}$

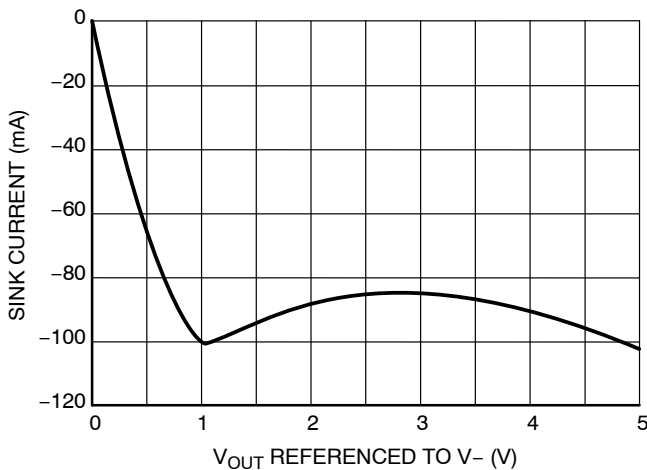


Figure 17. Sink Current vs. Output Voltage
 $V_S = 5.0\text{ V}$

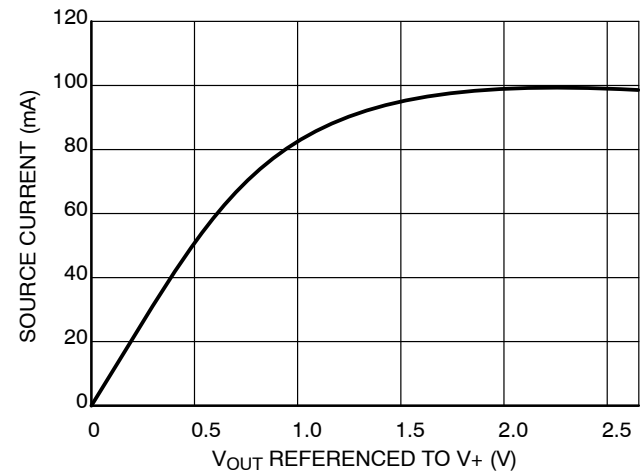


Figure 18. Source Current vs. Output Voltage
 $V_S = 2.7\text{ V}$

LMV321, NCV321, LMV358, LMV324

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)

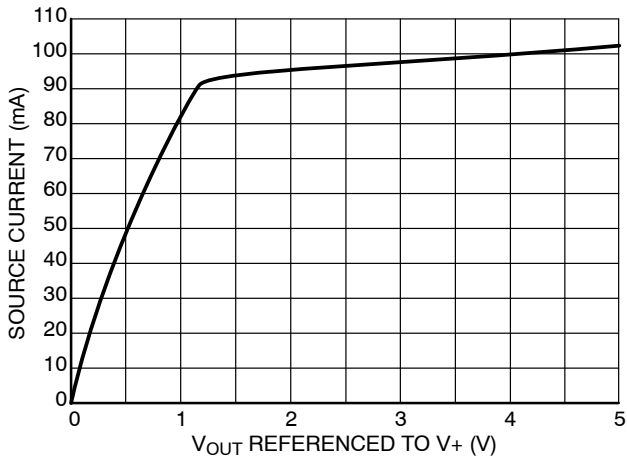


Figure 19. Source Current vs. Output Voltage
 $V_S = 5.0\text{ V}$

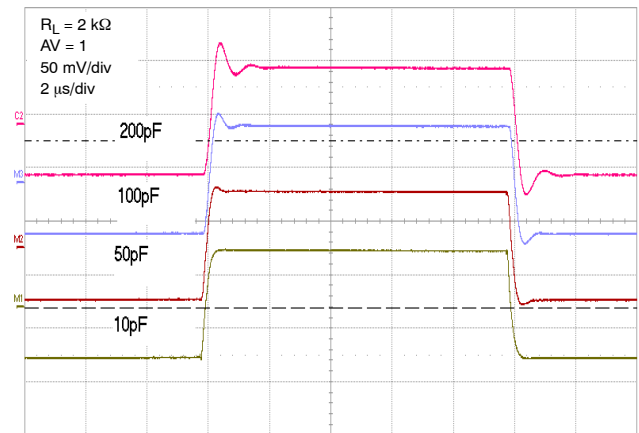


Figure 20. Settling Time vs. Capacitive Load

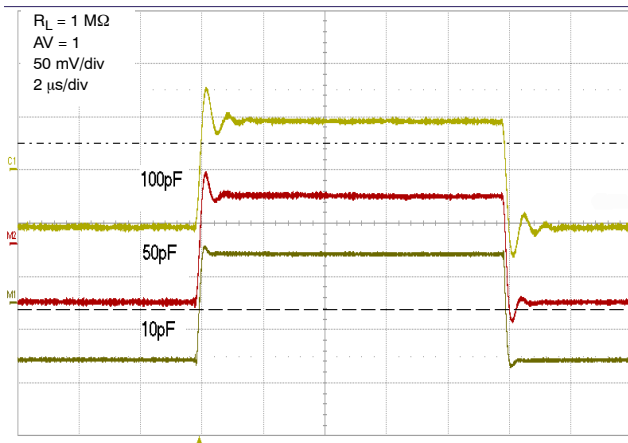


Figure 21. Settling Time vs. Capacitive Load

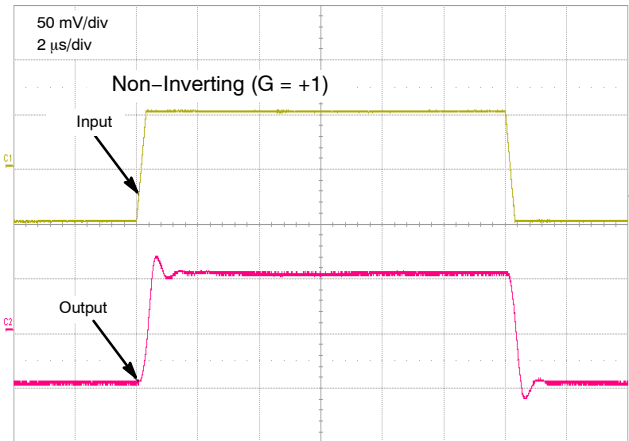


Figure 22. Step Response - Small Signal

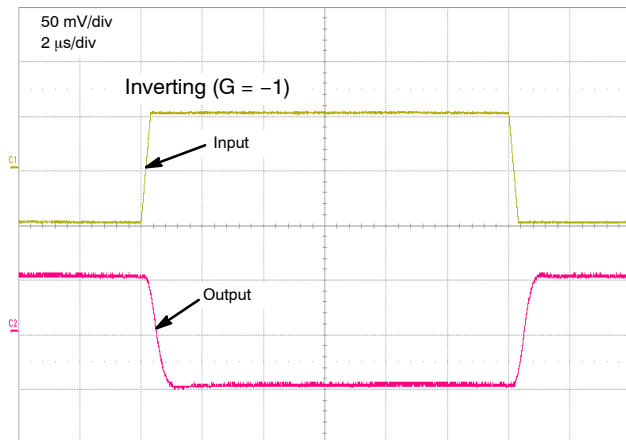


Figure 23. Step Response - Small Signal

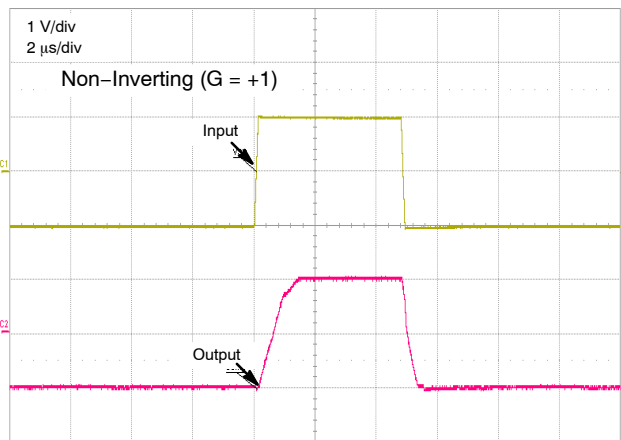


Figure 24. Step Response - Large Signal

LMV321, NCV321, LMV358, LMV324

TYPICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ and $V_S = 5\text{ V}$ unless otherwise specified)



Figure 25. Step Response – Large Signal

APPLICATIONS

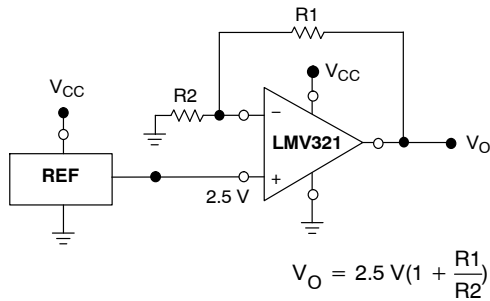


Figure 26. Voltage Reference

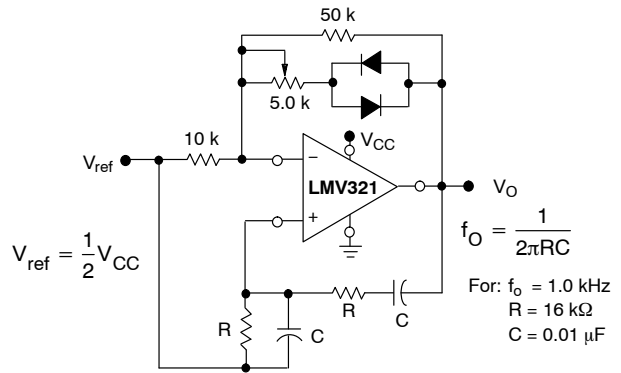


Figure 27. Wien Bridge Oscillator

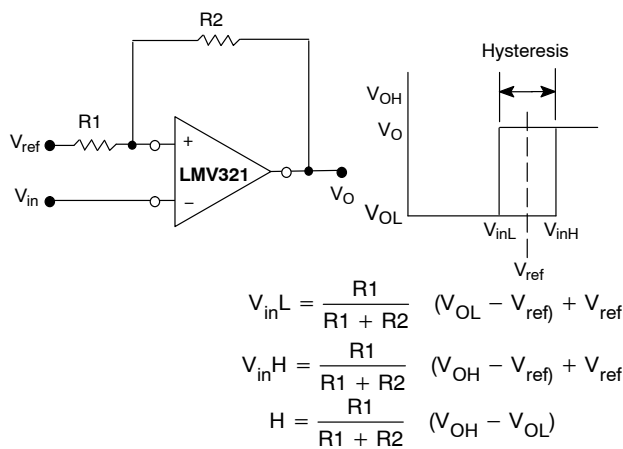
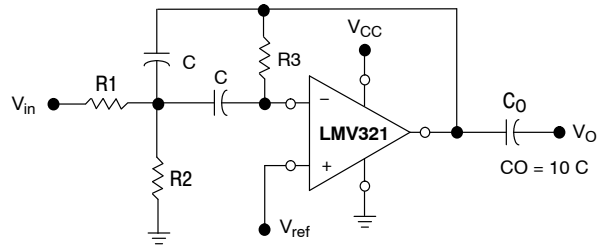


Figure 28. Comparator with Hysteresis



Given: f_o = center frequency
 $A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R_3 = \frac{Q}{\pi f_o C}$

$$R_1 = \frac{R_3}{2 A(f_o)}$$

$$R_2 = \frac{R_1 R_3}{4Q^2 R_1 - R_3}$$

For less than 10% error from operational amplifier,
 $((Q_o f_o)/BW) < 0.1$ where f_o and BW are expressed in Hz.
 If source impedance varies, filter may be preceded with
 voltage follower buffer to stabilize filter parameters.

Figure 29. Multiple Feedback Bandpass Filter

LMV321, NCV321, LMV358, LMV324

ORDERING INFORMATION

| Order Number | Number of Channels | Specific Device Marking | Package Type | Shipping† |
|---------------|--------------------|-------------------------|-----------------------|--------------------|
| LMV321SQ3T2G | Single | AAC | SC-70 (Pb-Free) | 3000 / Tape & Reel |
| LMV321SN3T1G | Single | 3AC | TSOP-5 (Pb-Free) | 3000 / Tape & Reel |
| LMV321ISN3T1G | Single | 3AC | TSOP-5 (Pb-Free) | 3000 / Tape & Reel |
| NCV321SN3T1G* | Single | 3AC | TSOP-5 (Pb-Free) | 3000 / Tape & Reel |
| LMV358DMR2G | Dual | V358 | Micro8 (Pb-Free) | 4000 / Tape & Reel |
| LMV358MUTAG | Dual | AC | UDFN8 (Pb-Free) | 3000 / Tape & Reel |
| LMV358DR2G | Dual | V358 | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| LMV358IDR2G | Dual | V358 | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| LMV324DR2G | Quad | LMV324 | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| LMV324DTBR2G | Quad | LMV324 | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

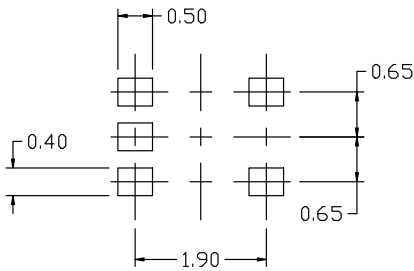
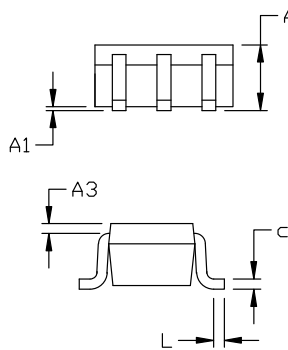
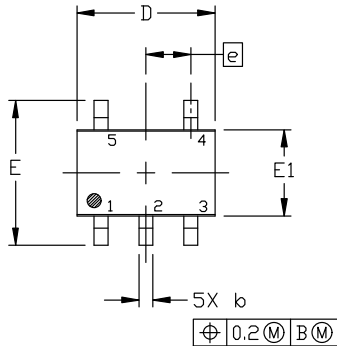
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED
MOUNTING FOOTPRINT

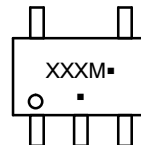
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 2:

- PIN 1. ANODE
- EMITTER
- BASE
- COLLECTOR
- CATHODE

STYLE 3:

- PIN 1. ANODE 1
- N/C
- ANODE 2
- CATHODE 2
- CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- DRAIN 1/2
- SOURCE 1
- GATE 1
- GATE 2

STYLE 5:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- BASE 2
- EMITTER 1
- COLLECTOR
- COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- COLLECTOR
- N/C
- BASE
- EMITTER

STYLE 9:

- PIN 1. ANODE
- CATHODE
- ANODE
- ANODE
- ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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| DESCRIPTION: | SC-88A (SC-70-5/SOT-353) | PAGE 1 OF 1 |

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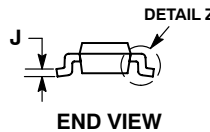
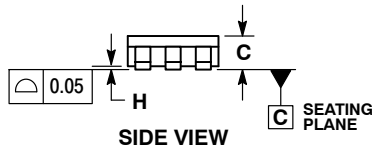
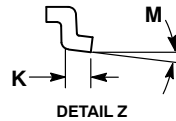
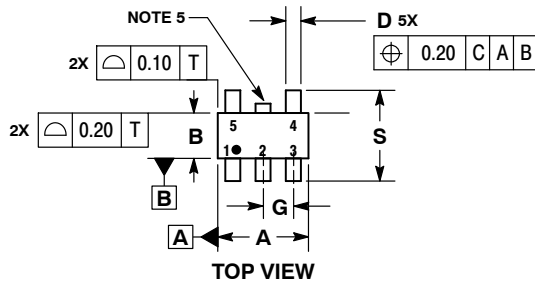
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

TSOP-5
CASE 483
ISSUE N

DATE 12 AUG 2020

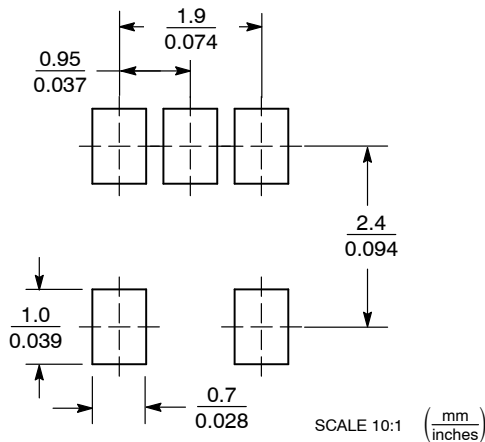


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

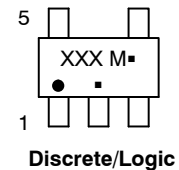
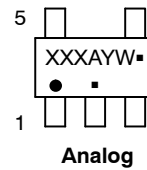
| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 2.85 | 3.15 |
| B | 1.35 | 1.65 |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0° | 10° |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ■ = Pb-Free Package
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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| DESCRIPTION: | TSOP-5 | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



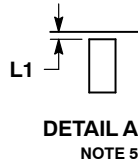
SCALE 4:1

UDFN8 1.8x1.2, 0.4P
CASE 517AJ-01
ISSUE O

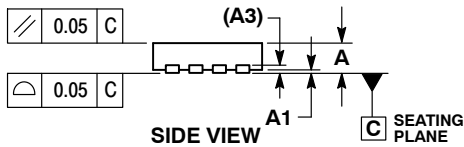
DATE 08 NOV 2006



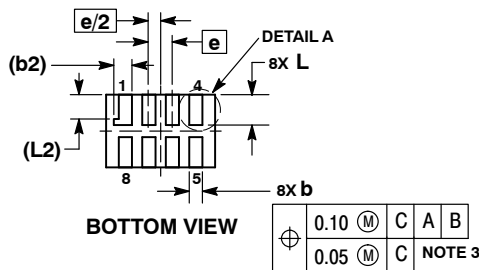
TOP VIEW



DETAIL A
NOTE 5



SIDE VIEW



BOTTOM VIEW

| | | | | | |
|---|------|-----|---|---|---|
| ⊕ | 0.10 | (M) | C | A | B |
| | 0.05 | (M) | C | | |

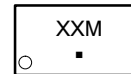
NOTE 3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

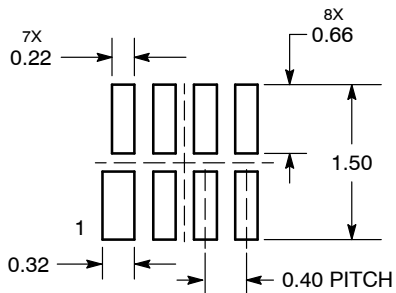
| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 | REF |
| b | 0.15 | 0.25 |
| b2 | 0.30 | REF |
| D | 1.80 | BSC |
| E | 1.20 | BSC |
| e | 0.40 | BSC |
| L | 0.45 | 0.55 |
| L1 | 0.00 | 0.03 |
| L2 | 0.40 | REF |

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

MOUNTING FOOTPRINT
SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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| DESCRIPTION: | UDFN8 1.8X1.2, 0.4P | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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| DESCRIPTION: | SOIC-8 NB | PAGE 2 OF 2 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

| DIM | MILLIMETERS | | |
|----------------------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| <i>b</i> | 0.25 | 0.33 | 0.40 |
| <i>c</i> | 0.13 | 0.18 | 0.23 |
| <i>D</i> | 2.90 | 3.00 | 3.10 |
| <i>E</i> | 2.90 | 3.00 | 3.10 |
| <i>e</i> | 0.65 BSC | | |
| <i>H_E</i> | 4.75 | 4.90 | 5.05 |
| <i>L</i> | 0.40 | 0.55 | 0.70 |



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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| DESCRIPTION: | MICRO8 | PAGE 1 OF 1 |

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