

# MC33078, MC33079, NCV33078, NCV33079

## Operational Amplifiers, Low Noise, Dual and Quad

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions and is available in the plastic DIP and SOIC packages (P and D suffixes).

### Features

- Dual Supply Operation:  $\pm 5.0$  V to  $\pm 18$  V
- Low Voltage Noise:  $4.5$  nV/ $\sqrt{\text{Hz}}$
- Low Input Offset Voltage:  $0.15$  mV
- Low T.C. of Input Offset Voltage:  $2.0$   $\mu\text{V}/^\circ\text{C}$
- Low Total Harmonic Distortion:  $0.002\%$
- High Gain Bandwidth Product:  $16$  MHz
- High Slew Rate:  $7.0$  V/ $\mu\text{s}$
- High Open Loop AC Gain:  $800$  @  $20$  kHz
- Excellent Frequency Stability
- Large Output Voltage Swing:  $+14.1$  V/  $-14.6$  V
- ESD Diodes Provided on the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

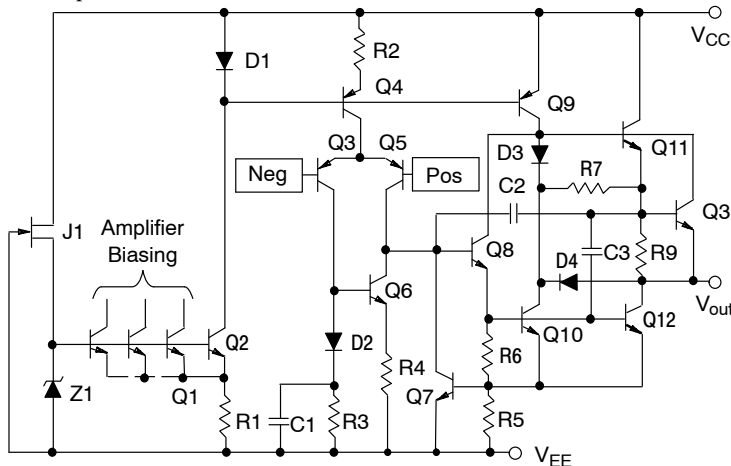


Figure 1. Representative Schematic Diagram  
(Each Amplifier)

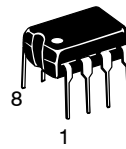


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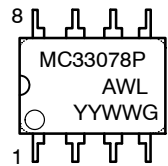
<http://onsemi.com>

### MARKING DIAGRAMS

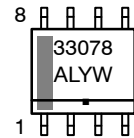
#### DUAL



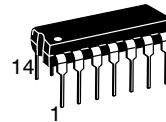
PDIP-8  
P SUFFIX  
CASE 626



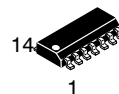
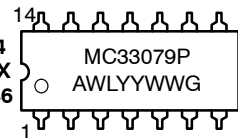
SOIC-8  
D SUFFIX  
CASE 751



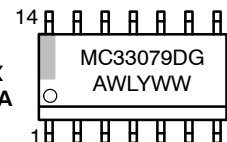
#### QUAD



PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



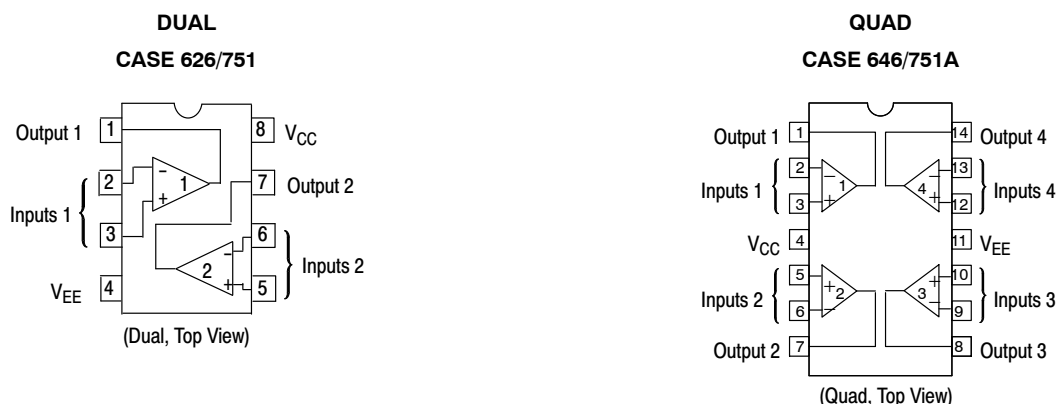
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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## PIN CONNECTIONS



### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage ( $V_{CC}$ to $V_{EE}$ )	$V_S$	+36	V
Input Differential Voltage Range	$V_{IDR}$	Note 1	V
Input Voltage Range	$V_{IR}$	Note 1	V
Output Short Circuit Duration (Note 2)	$t_{SC}$	Indefinite	sec
Maximum Junction Temperature	$T_J$	+150	°C
Storage Temperature	$T_{stg}$	-60 to +150	°C
ESD Protection at any Pin MC33078/NCV33078 MC33079/NCV33079	$V_{esd}$	600 200 550 150	V
Maximum Power Dissipation	$P_D$	Note 2	mW
Operating Temperature Range	$T_A$	-40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages must not exceed the magnitude of  $V_{CC}$  or  $V_{EE}$ .
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded (see Figure 2).

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**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

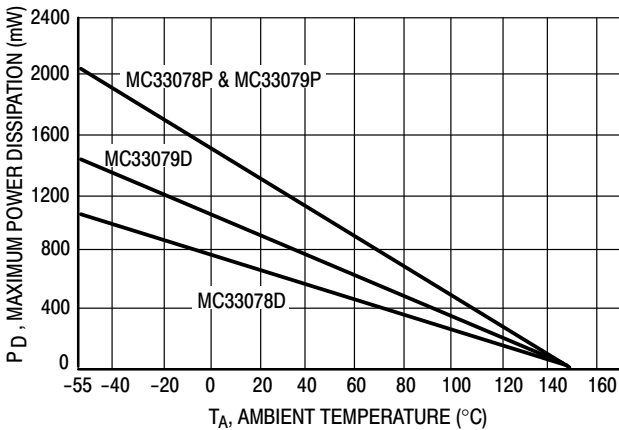
Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ( $R_S = 10\ \Omega$ , $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) (MC33078) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ (MC33079) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$ V_{IO} $	-	0.15	2.0	mV
		-	-	3.0	
		-	0.15	2.5	
		-	-	3.5	
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$ , $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $T_A = T_{low}$ to $T_{high}$	$\Delta V_{IO}/\Delta T$	-	2.0	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$I_{IB}$	-	300	750	nA
		-	-	800	
Input Offset Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$I_{IO}$	-	25	150	nA
		-	-	175	
Common Mode Input Voltage Range ( $\Delta V_{IO} = 5.0\text{ mV}$ , $V_O = 0\text{ V}$ )	$V_{ICR}$	$\pm 13$	$\pm 14$	-	V
Large Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ ) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$A_{VOL}$	90	110	-	dB
		85	-	-	
Output Voltage Swing ( $V_{ID} = \pm 1.0\text{ V}$ ) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$	$V_{O+}$ $V_{O-}$ $V_{O+}$ $V_{O-}$ $V_{O+}$ $V_{O-}$	-	+10.7	-	V
		-	-11.9	-	
		+13.2	+13.8	-	
		-	-13.7	-13.2	
		+13.5	+14.1	-	
		-	-14.6	-14	
Common Mode Rejection ( $V_{in} = \pm 13\text{ V}$ )	CMR	80	100	-	dB
Power Supply Rejection (Note 3) $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$ to $+5.0\text{ V}/-5.0\text{ V}$	PSR	80	105	-	dB
Output Short Circuit Current ( $V_{ID} = 1.0\text{ V}$ , Output to Ground) Source Sink	$I_{SC}$	+15 -20	+29 -37	- -	mA
Power Supply Current ( $V_O = 0\text{ V}$ , All Amplifiers) (MC33078) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ (MC33079) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$I_D$	-	4.1	5.0	mA
		-	-	5.5	
		-	8.4	10	
		-	-	11	

3. Measured with  $V_{CC}$  and  $V_{EE}$  differentially varied simultaneously.

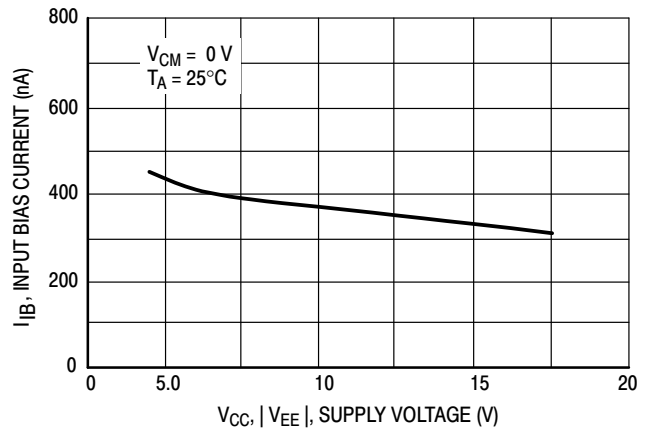
# MC33078, MC33079, NCV33078, NCV33079

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

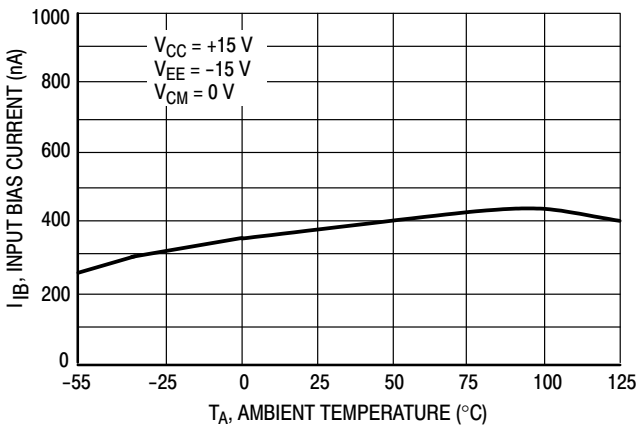
Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ( $V_{in} = -10\text{ V to } +10\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = +1.0$ )	SR	5.0	7.0	–	V/ $\mu\text{s}$
Gain Bandwidth Product ( $f = 100\text{ kHz}$ )	GBW	10	16	–	MHz
Unity Gain Bandwidth (Open Loop)	BW	–	9.0	–	MHz
Gain Margin ( $R_L = 2.0\text{ k}\Omega$ $C_L = 0\text{ pF}$ $C_L = 100\text{ pF}$ )	$A_m$	– –	–11 –6.0	– –	dB
Phase Margin ( $R_L = 2.0\text{ k}\Omega$ $C_L = 0\text{ pF}$ $C_L = 100\text{ pF}$ )	$\phi_m$	– –	55 40	– –	Deg
Channel Separation ( $f = 20\text{ Hz to } 20\text{ kHz}$ )	CS	–	–120	–	dB
Power Bandwidth ( $V_O = 27\text{ V}_{pp}$ , $R_L = 2.0\text{ k}\Omega$ , THD $\pm 1.0\%$ )	$BW_p$	–	120	–	kHz
Total Harmonic Distortion ( $R_L = 2.0\text{ k}\Omega$ , $f = 20\text{ Hz to } 20\text{ kHz}$ , $V_O = 3.0\text{ V}_{rms}$ , $A_V = +1.0$ )	THD	–	0.002	–	%
Open Loop Output Impedance ( $V_O = 0\text{ V}$ , $f = 9.0\text{ MHz}$ )	$ Z_O $	–	37	–	$\Omega$
Differential Input Resistance ( $V_{CM} = 0\text{ V}$ )	$R_{in}$	–	175	–	$\text{k}\Omega$
Differential Input Capacitance ( $V_{CM} = 0\text{ V}$ )	$C_{in}$	–	12	–	pF
Equivalent Input Noise Voltage ( $R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$ )	$e_n$	–	4.5	–	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ( $f = 1.0\text{ kHz}$ )	$i_n$	–	0.5	–	$\text{Hz}\sqrt{\text{pA}}$



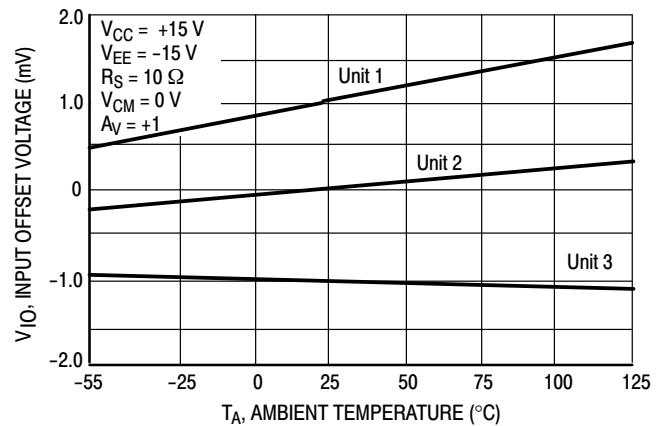
**Figure 2. Maximum Power Dissipation versus Temperature**



**Figure 3. Input Bias Current versus Supply Voltage**



**Figure 4. Input Bias Current versus Temperature**



**Figure 5. Input Offset Voltage versus Temperature**

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Figure 6. Input Bias Current versus Common Mode Voltage

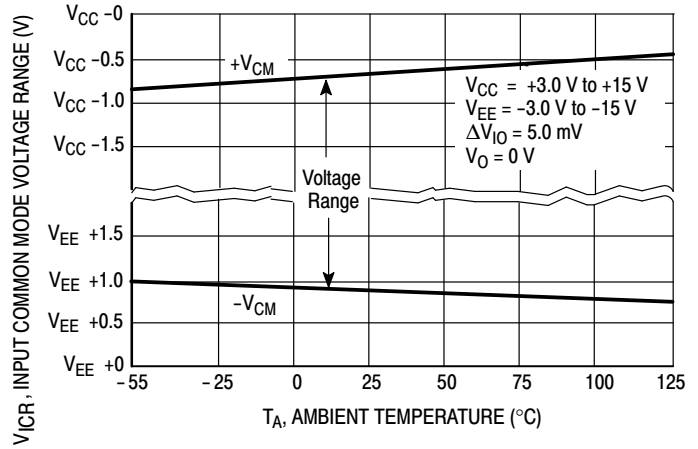


Figure 7. Input Common Mode Voltage Range versus Temperature



Figure 8. Output Saturation Voltage versus Load Resistance to Ground



Figure 9. Output Short Circuit Current versus Temperature



Figure 10. Supply Current versus Temperature

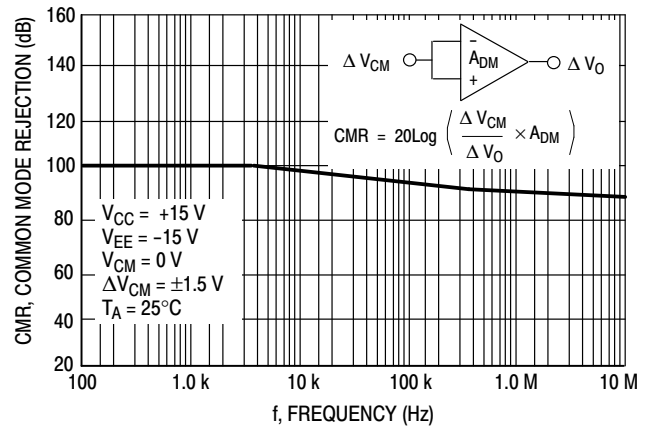


Figure 11. Common Mode Rejection versus Frequency

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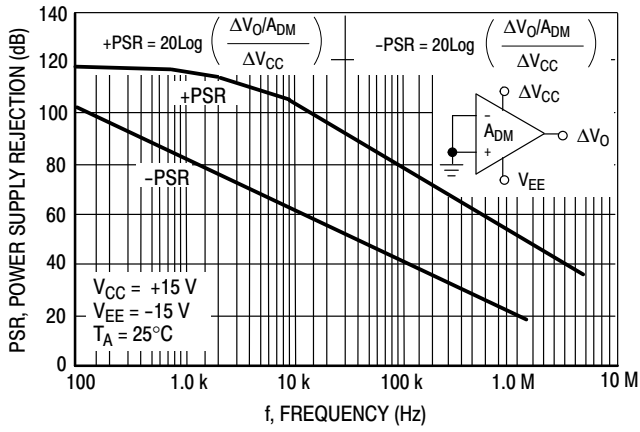


Figure 12. Power Supply Rejection versus Frequency

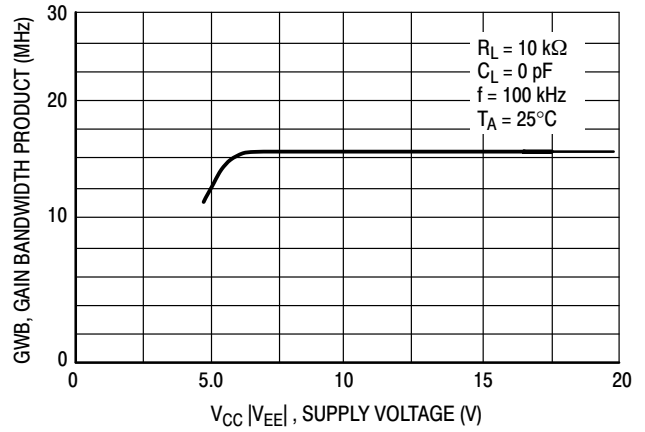


Figure 13. Gain Bandwidth Product versus Supply Voltage

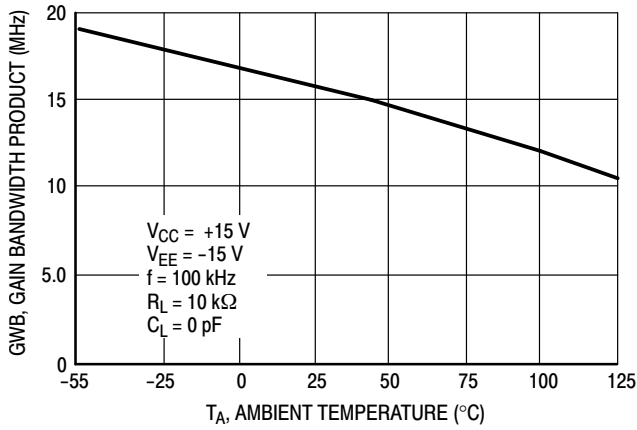


Figure 14. Gain Bandwidth Product versus Temperature

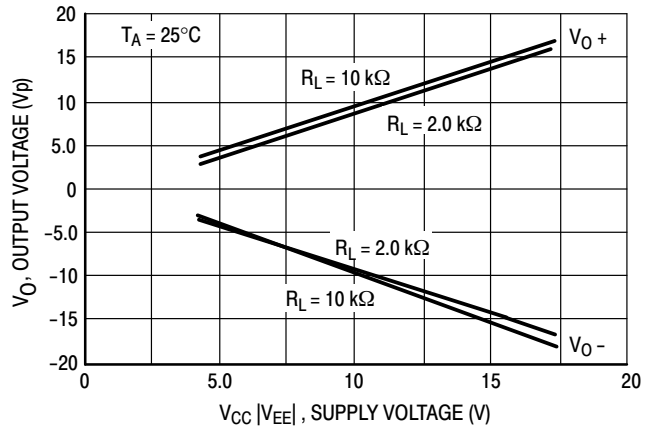


Figure 15. Maximum Output Voltage versus Supply Voltage

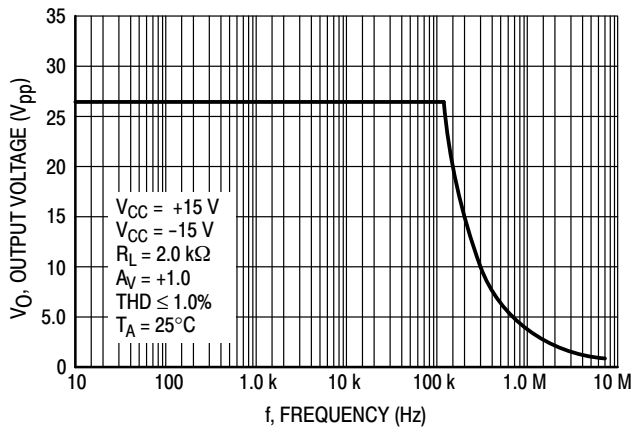


Figure 16. Output Voltage versus Frequency

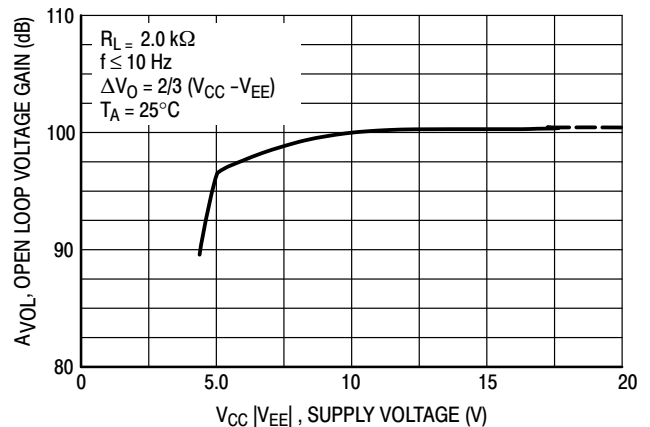


Figure 17. Open Loop Voltage Gain versus Supply Voltage

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Figure 18. Open Loop Voltage Gain versus Temperature



Figure 19. Output Impedance versus Frequency



Figure 20. Channel Separation versus Frequency



Figure 21. Total Harmonic Distortion versus Frequency

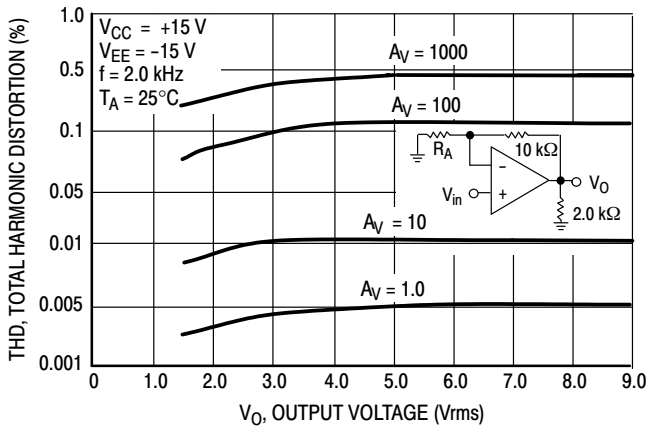


Figure 22. Total Harmonic Distortion versus Output Voltage

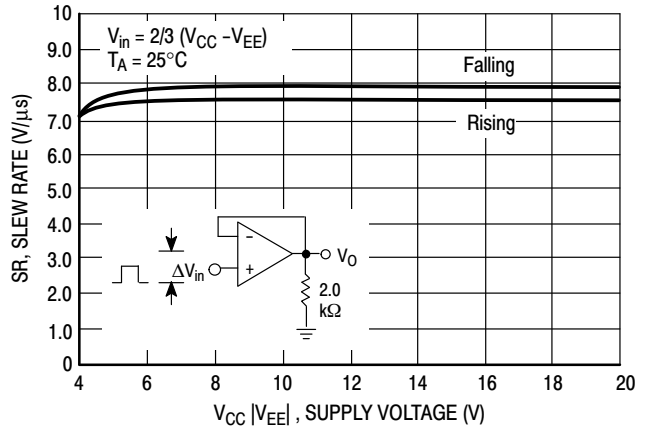


Figure 23. Slew Rate versus Supply Voltage

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Figure 24. Slew Rate versus Temperature

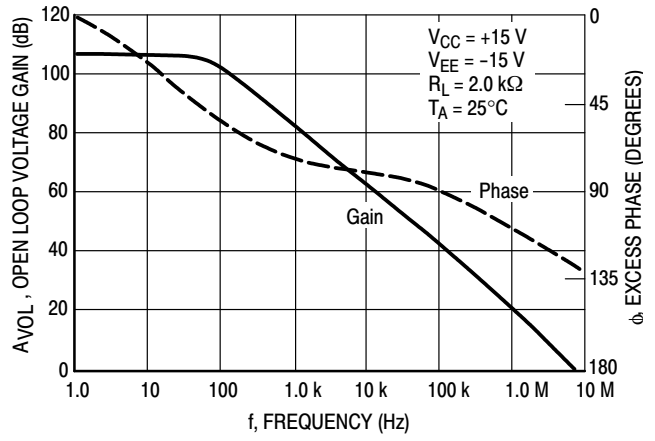


Figure 25. Voltage Gain and Phase versus Frequency



Figure 26. Open Loop Gain Margin and Phase Margin versus Load Capacitance

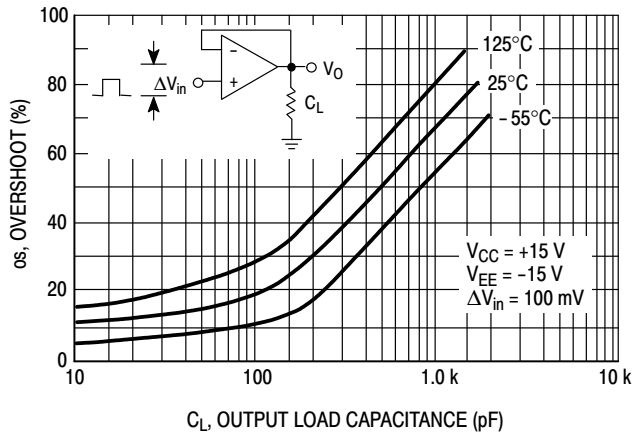


Figure 27. Overshoot versus Output Load Capacitance

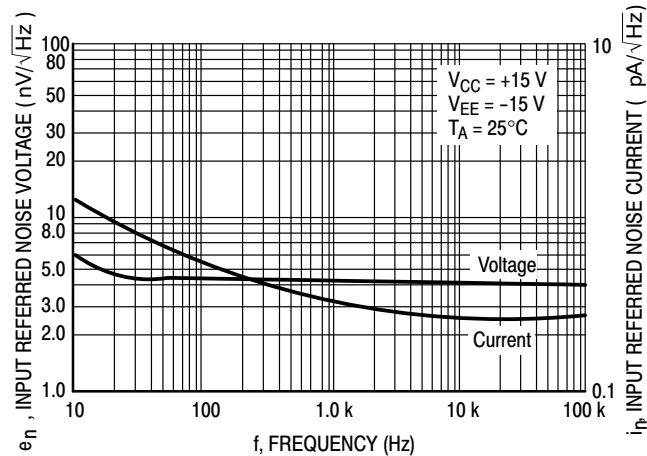


Figure 28. Input Referred Noise Voltage and Current versus Frequency

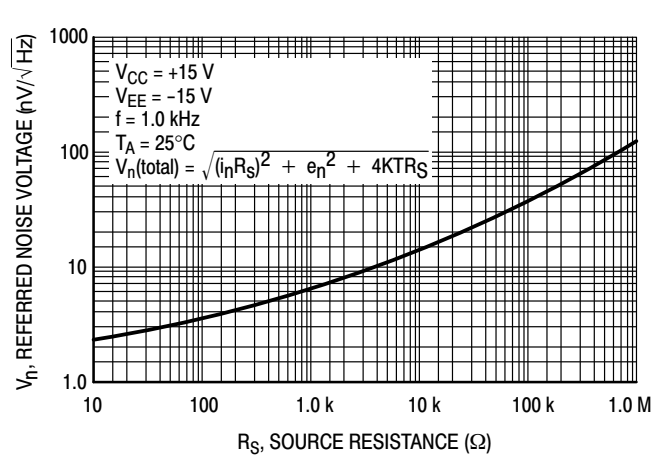


Figure 29. Total Input Referred Noise Voltage versus Source Resistance



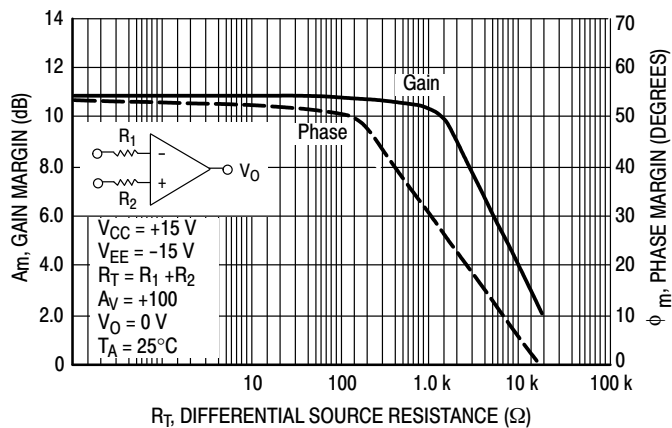


Figure 30. Phase Margin and Gain Margin versus Differential Source Resistance

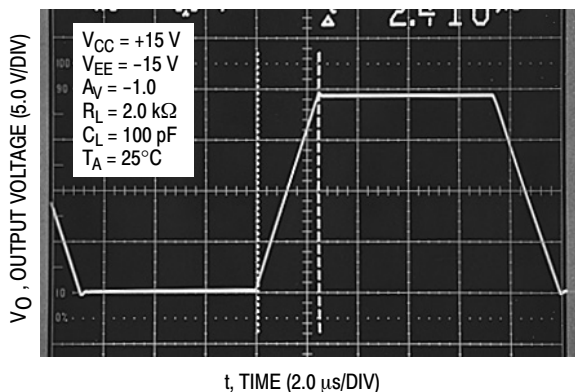


Figure 31. Inverting Amplifier Slew Rate

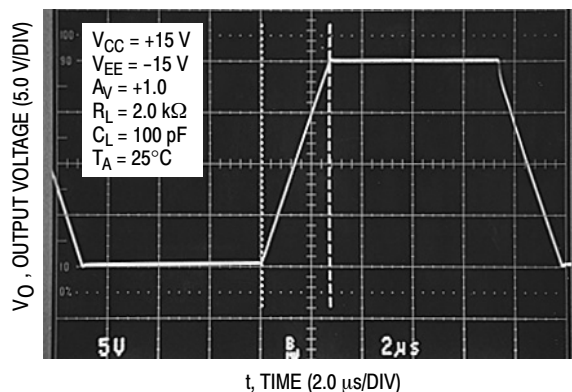


Figure 32. Non-inverting Amplifier Slew Rate

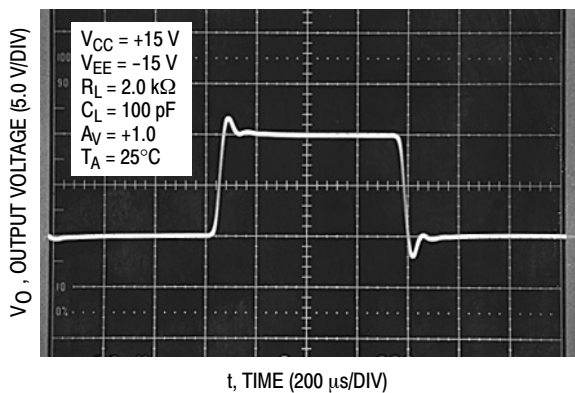


Figure 33. Non-inverting Amplifier Overshoot

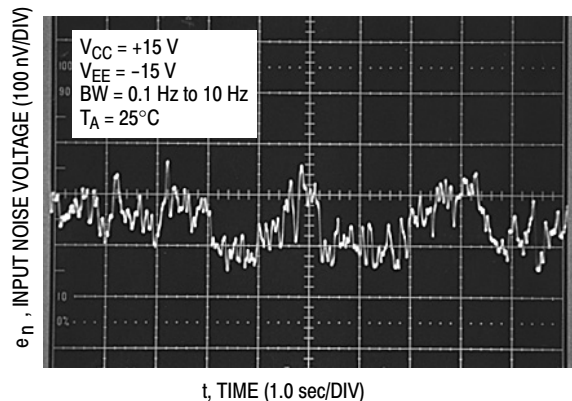
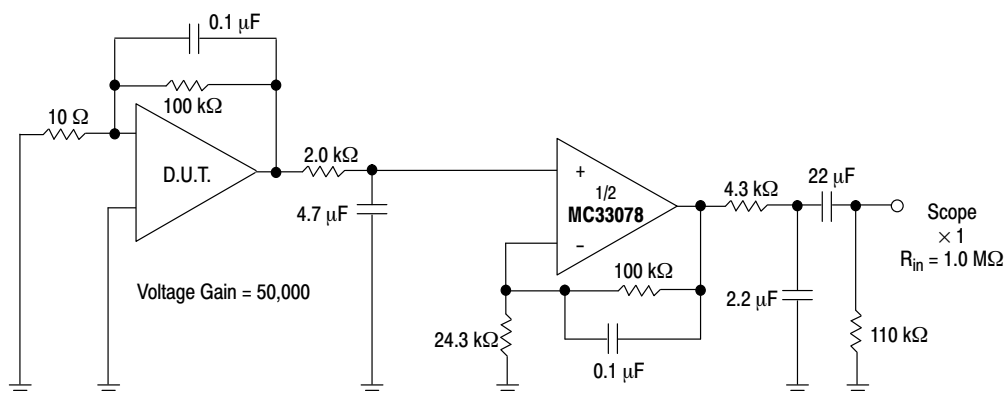


Figure 34. Low Frequency Noise Voltage versus Time

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Note: All capacitors are non-polarized.

**Figure 35. Voltage Noise Test Circuit  
(0.1 Hz to 10 Hz<sub>p-p</sub>)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC33078DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33078DR2G		2500 / Tape & Reel
NCV33078DR2G*		
MC33078P	PDIP-8	50 Units / Rail
MC33078PG	PDIP-8 (Pb-Free)	
MC33079DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC33079DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NCV33079DR2G*		
MC33079P	PDIP-14	25 Units / Rail
MC33079PG	PDIP-14 (Pb-Free)	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV devices are qualified for automotive use.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

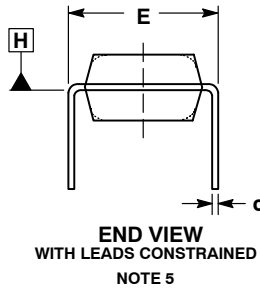
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SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

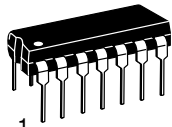
- STYLE 1:  
PIN 1. AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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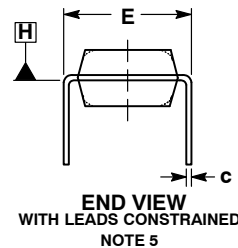


SCALE 1:1



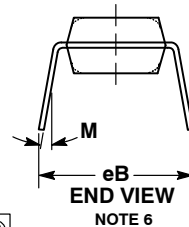
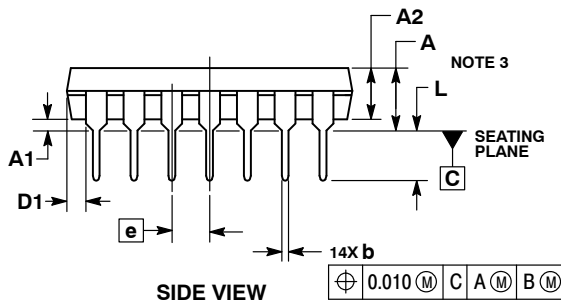
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ISSUE S

DATE 22 APR 2015



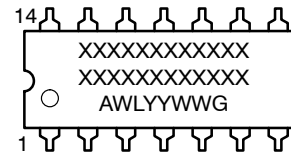
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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DESCRIPTION:	PDIP-14	PAGE 1 OF 2

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**PDIP-14**  
**CASE 646-06**  
**ISSUE S**

DATE 22 APR 2015

STYLE 1:  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER  
 4. NO  
 CONNECTION  
 5. EMITTER  
 6. BASE  
 7. COLLECTOR  
 8. COLLECTOR  
 9. BASE  
 10. EMITTER  
 11. NO  
 CONNECTION  
 12. EMITTER  
 13. BASE  
 14. COLLECTOR

STYLE 2:  
 CANCELLED

STYLE 3:  
 CANCELLED

STYLE 4:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE  
 4. NO  
 CONNECTION  
 5. GATE  
 6. SOURCE  
 7. DRAIN  
 8. DRAIN  
 9. SOURCE  
 10. GATE  
 11. NO  
 CONNECTION  
 12. GATE  
 13. SOURCE  
 14. DRAIN

STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. NO CONNECTION  
 5. SOURCE  
 6. DRAIN  
 7. GATE  
 8. GATE  
 9. DRAIN  
 10. SOURCE  
 11. NO CONNECTION  
 12. SOURCE  
 13. DRAIN  
 14. GATE

STYLE 6:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 7:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON  
 CATHODE

STYLE 8:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 9:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

STYLE 10:  
 PIN 1. COMMON  
 CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON  
 CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 11:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 12:  
 PIN 1. COMMON CATHODE  
 2. COMMON ANODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. COMMON ANODE  
 7. COMMON CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*

### SOLDERING FOOTPRINT\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC_OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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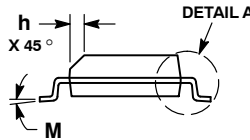
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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