NCP2890, NCV2890

Audio Power Amplifier, 1.0 W

The NCP2890 is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The NCP2890 is capable of delivering 1.0 W of continuous average power to an 8.0 ΩBTL load from a 5.0 V power supply, and 320 mW to a 4.0 Ω BTL load from a 2.6 V power supply.

The NCP2890 provides high quality audio while requiring few external components and minimal power consumption. It features a low−power consumption shutdown mode, which is achieved by driving the SHUTDOWN pin with logic low

The NCP2890 contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn−on and turn−off transitions.

For maximum flexibility, the NCP2890 provides an externally controlled gain (with resistors), as well as an externally controlled turn−on time (with the bypass capacitor).

Due to its excellent PSRR, it can be directly connected to the battery, saving the use of an LDO.

This device is available in a 9−Pin Flip−Chip CSP (standard −Lead and Lead−Free versions) and a Micro8™ package.

Features

- 1.0 W to an 8.0 Ω BTL Load from a 5.0 V Power Supply
- Excellent PSRR: Direct Connection to the Battery
- “Pop and Click” Noise Protection Circuit
- Ultra Low Current Shutdown Mode
- 2.2 V−5.5 V Operation
- External Gain Configuration Capability
- External Turn−on Time Configuration Capability
- Up to 1.0 nF Capacitive Load Driving Capability
- Thermal Overload Protection Circuitry
- AEC−Q100 Qualified Part Available
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

Typical Applications

- Portable Electronic Devices
- PDAs
- Wireless Phones

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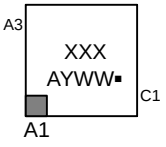
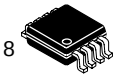
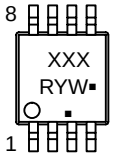
MARKING DIAGRAMS

9−Pin Flip−Chip CSP
FC SUFFIX
CASE 499E





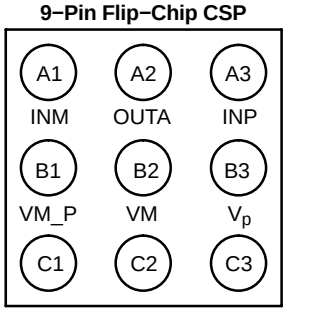
Micro8
DM SUFFIX
CASE 846A



XXX = Specific Device Code,
A, R = Assembly Location
Y = Year
WW, W = Work Week
▪ = Pb−Free Package

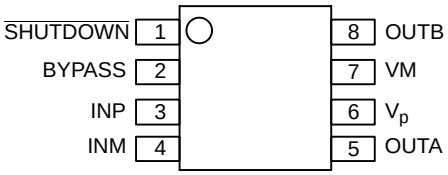
PIN CONNECTIONS

9−Pin Flip−Chip CSP



(Top View)

Micro8



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

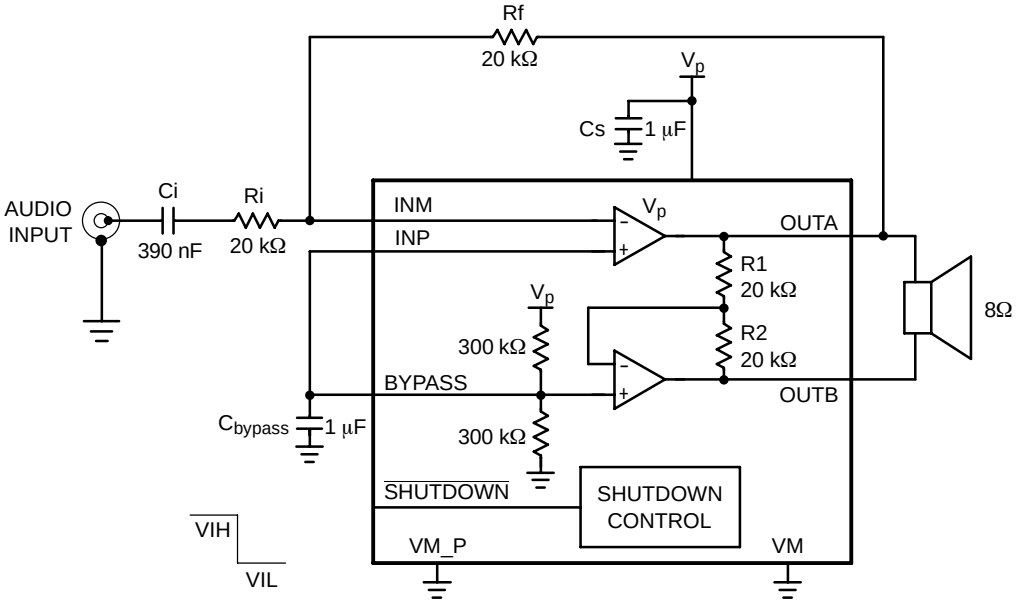


Figure 1. Typical Audio Amplifier Application Circuit with Single Ended Input

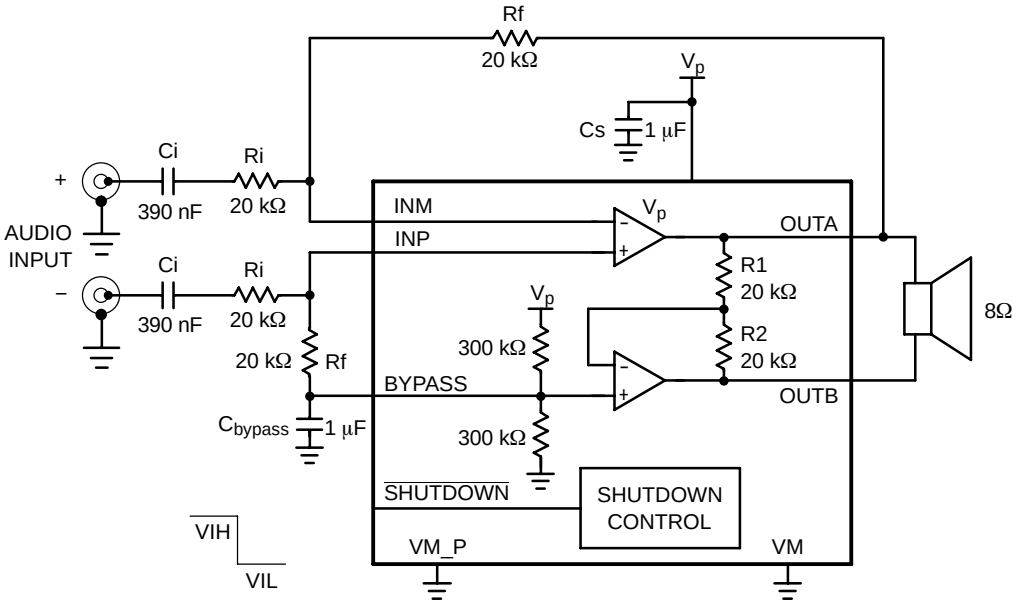


Figure 2. Typical Audio Amplifier Application Circuit with a Differential Input

This device contains 671 active transistors and 1899 MOS gates.

PIN DESCRIPTION

9−Pin Flip−Chip CSP	Micro8	Type	Symbol	Description
A1	4	I	INM	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_f and to the input resistor R_{in}.
A2	5	O	OUTA	Negative output of the NCP2890. Connected to the load and to the feedback resistor Rf.
A3	3	I	INP	Positive input of the first amplifier, receives the common mode voltage.
B1	NA	I	VM_P	Power Analog Ground.
B2	7	I	VM	Core Analog Ground.
B3	6	I	V_p	Positive analog supply of the cell. Range: 2.2 V−5.5 V.
C1	2	I	BYPASS	Bypass capacitor pin which provides the common mode voltage (Vp/2).
C2	8	O	OUTB	Positive output of the NCP2890. Connected to the load.
C3	1	I	$\overline{\text{SHUTDOWN}}$	The device enters in shutdown mode when a low level is applied on this pin.

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Supply Voltage		V_p	6.0	V
Operating Supply Voltage		Op Vp	2.2 to 5.5 V 2.0 V = Functional Only	−
Input Voltage		V_{in}	−0.3 to Vcc +0.3	V
Max Output Current		Iout	500	mA
Power Dissipation (Note 2)		Pd	Internally Limited	−
Operating Ambient Temperature		T_A	−40 to +85	°C
Max Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Thermal Resistance Junction−to−Air	Micro8 9−Pin Flip−Chip CSP	$R_{\theta JA}$	230 (Note 3)	°C/W
ESD Protection	Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)	−	8000 >250	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation. For further information see page 10.
3. For the 9−Pin Flip−Chip CSP package, the $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. For further information see page 10. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.
4. Human Body Model, 100 pF discharge through a 1.5 kΩ resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Supply Quiescent Current	I_{dd}	V_p = 2.6 V, No Load V_p = 5.0 V, No Load	− −	1.5 1.7	4	mA
		V_p = 2.6 V, 8 Ω V_p = 5.0 V, 8 Ω	− −	1.7 1.9	5.5	
Common Mode Voltage	V_{cm}	−	−	V_p/2	−	V
Shutdown Current	I_{SD}	−	−	10	600	nA
Shutdown Voltage High	V_{SDIH}	−	1.2	−	−	V
Shutdown Voltage Low	V_{SDIL}	−	−	−	0.4	V
Turning On Time (Note 8)	T_{WU}	C_{by} = 1 μF	−	285	−	ms
Output Swing	$V_{loadpeak}$	V_p = 2.6 V, R_L = 8.0 Ω V_p = 5.0 V, R_L = 8.0 Ω (Note 7)	2.0 4.0	2.12 4.15	− −	V
Rms Output Power	P_O	V_p = 2.6 V, R_L = 4.0 Ω THD + N < 0.1% V_p = 2.6 V, R_L = 8.0 Ω THD + N < 0.1% V_p = 5.0 V, R_L = 8.0 Ω THD + N < 0.1%	− −	0.36 0.28 1.08	− − 	W
Maximum Power Dissipation (Note 8)	P_{Dmax}	V_p = 5.0 V, R_L = 8.0 Ω	−	−	0.65	W
Output Offset Voltage	V_{OS}	V_p = 2.6 V V_p = 5.0 V	−30		30	mV
Signal−to−Noise Ratio	SNR	V_p = 2.6 V, G = 2.0 10 Hz < F < 20 kHz V_p = 5.0 V, G = 10 10 Hz < F < 20 kHz	− −	84 77	− −	dB
Positive Supply Rejection Ratio	PSRR V+	G = 2.0, R_L = 8.0 Ω Vp_{ripple_pp} = 200 mV C_{by} = 1.0 μF Input Terminated with 10 Ω F = 217 Hz V_p = 5.0 V V_p = 3.0 V V_p = 2.6 V F = 1.0 kHz V_p = 5.0 V V_p = 3.0 V V_p = 2.6 V	 − − − − − −	 −64 −72 −73 −64 −74 −75	 − − − − − −	dB
Efficiency	η	V_p = 2.6 V, P_{orms} = 320 mW V_p = 5.0 V, P_{orms} = 1.0 W	− −	48 63	− −	%
Thermal Shutdown Temperature (Note 9)	T_{sd}		140	160	180	°C
Total Harmonic Distortion	THD	V_p = 2.6, F = 1.0 kHz R_L = 4.0 Ω, A_V = 2.0 P_O = 0.32 W V_p = 5.0 V, F = 1.0 kHz R_L = 8.0 Ω, A_V = 2.0 P_O = 1.0 W	− − − − − −	− 0.04 − − 0.02 −	− − − − − −	%

6. Min/Max limits are guaranteed by design, test or statistical analysis.
7. This parameter is not tested in production for 9−Pin Flip−Chip CSP package in case of a 5.0 V power supply.
8. See page 11 for a theoretical approach of this parameter.
9. For this parameter, the Min/Max values are given for information.

TYPICAL PERFORMANCE CHARACTERISTICS

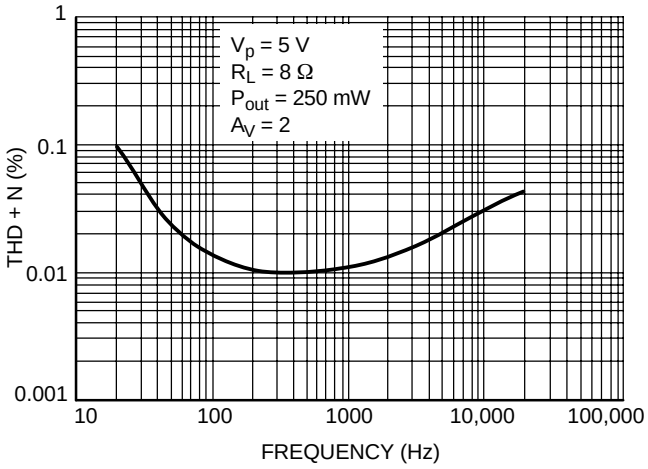


Figure 1. THD + N versus Frequency

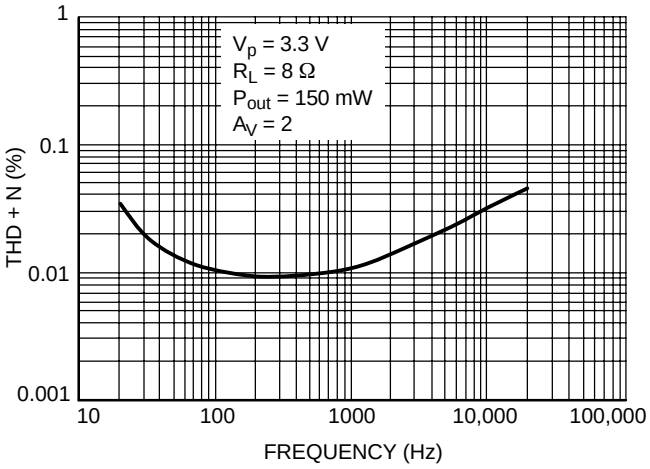


Figure 2. THD + N versus Frequency

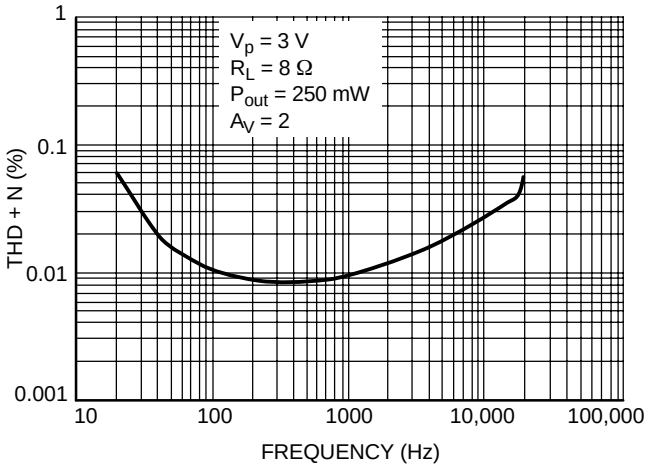


Figure 3. THD + N versus Frequency

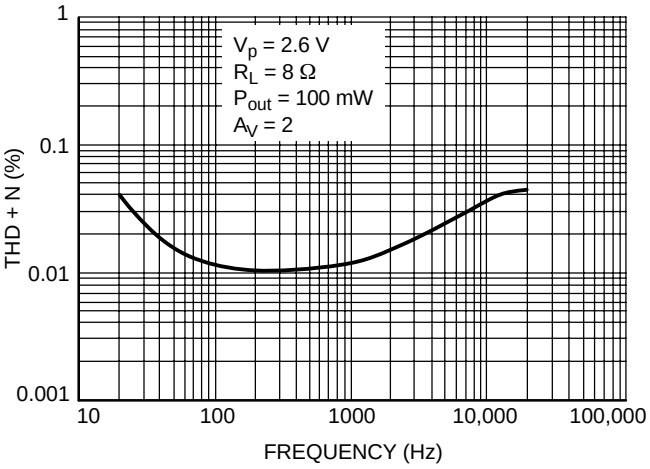


Figure 4. THD + N versus Frequency

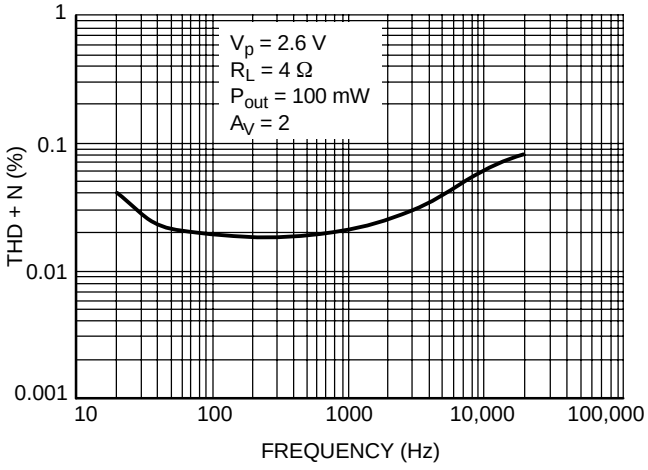


Figure 5. THD + N versus Frequency

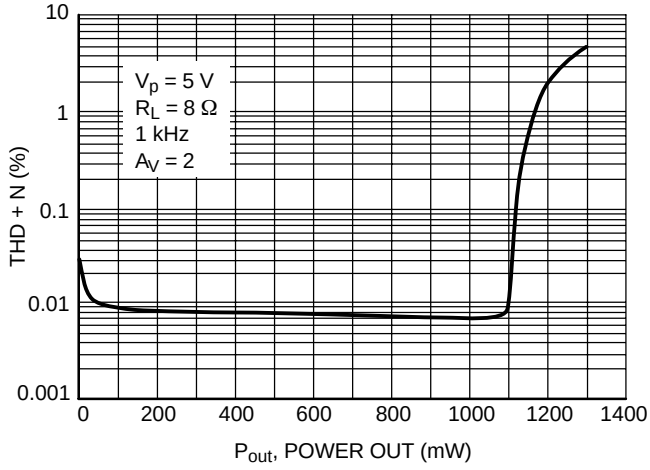


Figure 6. THD + N versus Power Out

TYPICAL PERFORMANCE CHARACTERISTICS

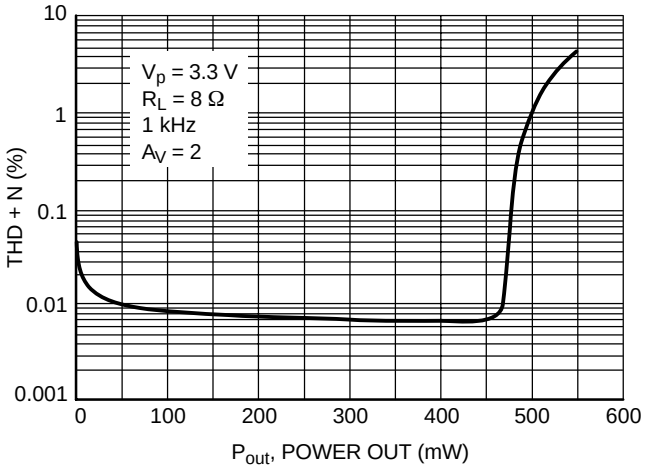


Figure 7. THD + N versus Power Out

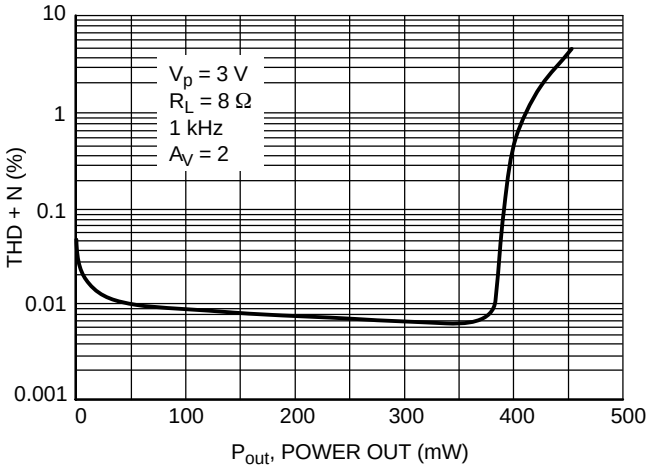


Figure 8. THD + N versus Power Out

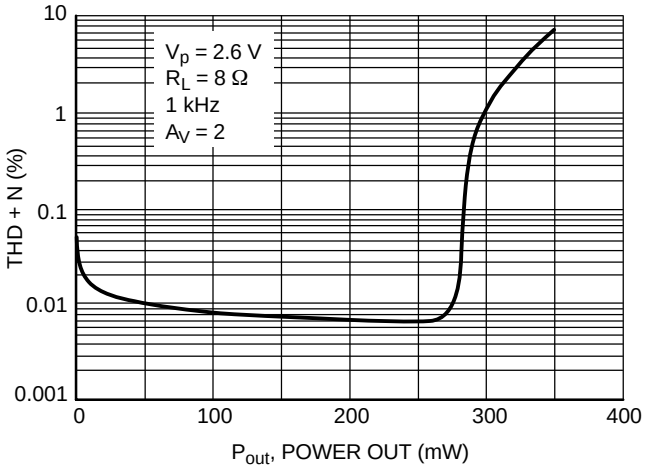


Figure 9. THD + N versus Power Out

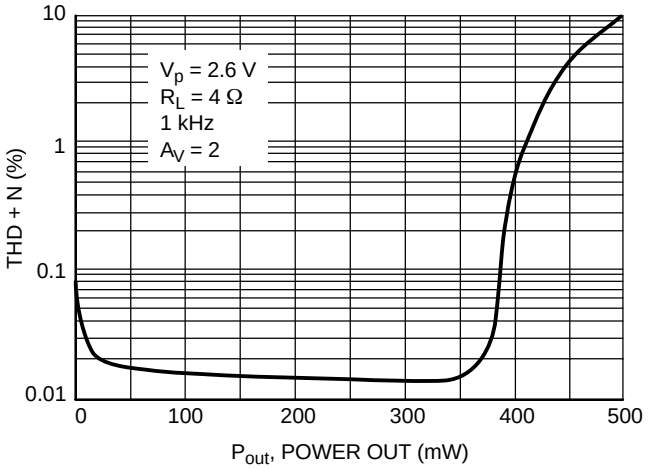


Figure 10. THD + N versus Power Out

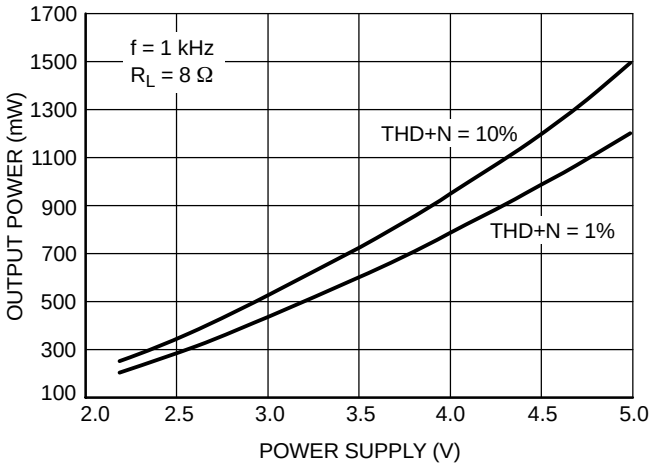


Figure 11. Output Power versus Power Supply

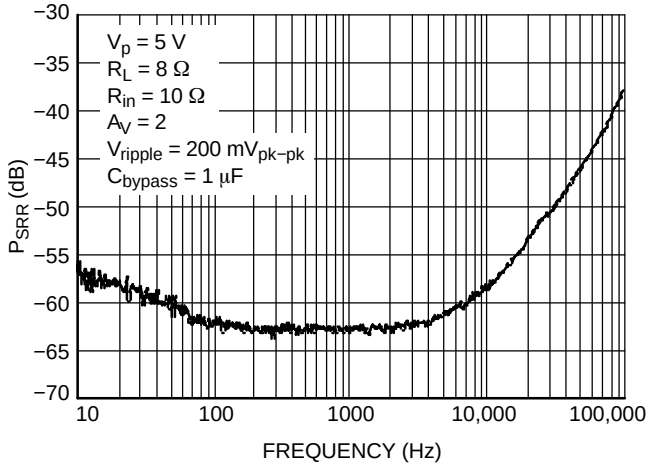


Figure 12. P_{SRR} @ V_p = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

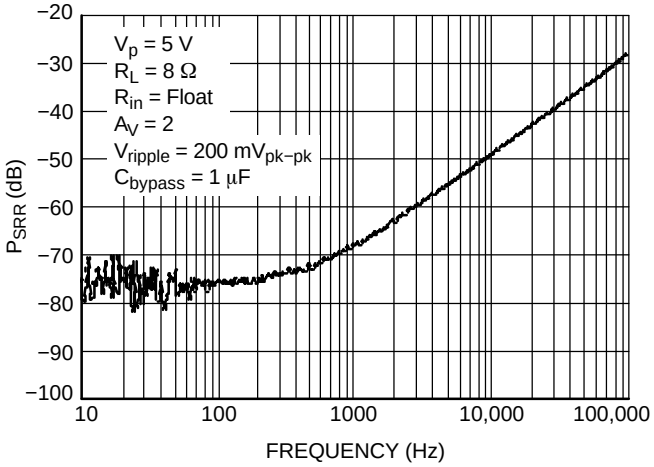


Figure 13. P_{SRR} @ V_p = 5 V

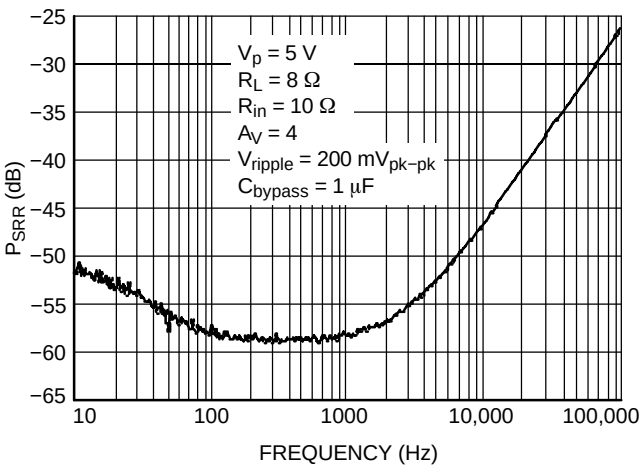


Figure 14. P_{SRR} @ V_p = 5 V

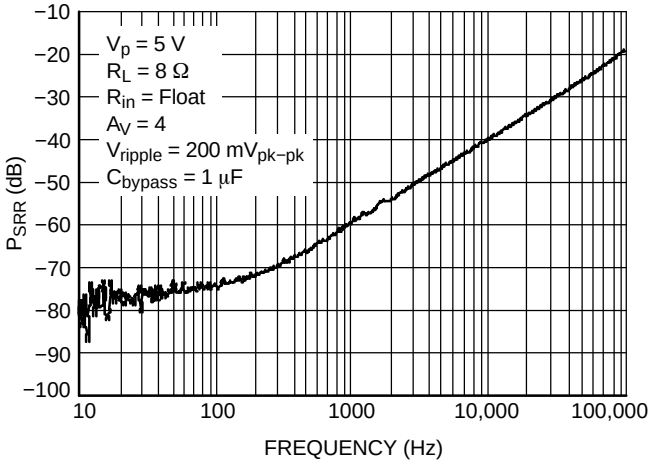


Figure 15. P_{SRR} @ V_p = 5 V

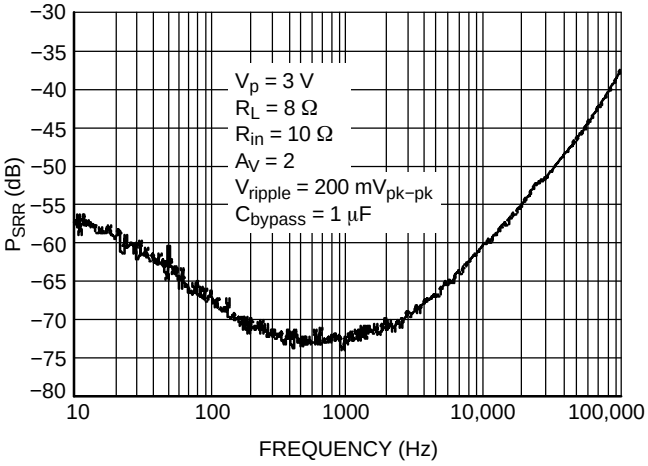


Figure 16. P_{SRR} @ V_p = 3 V

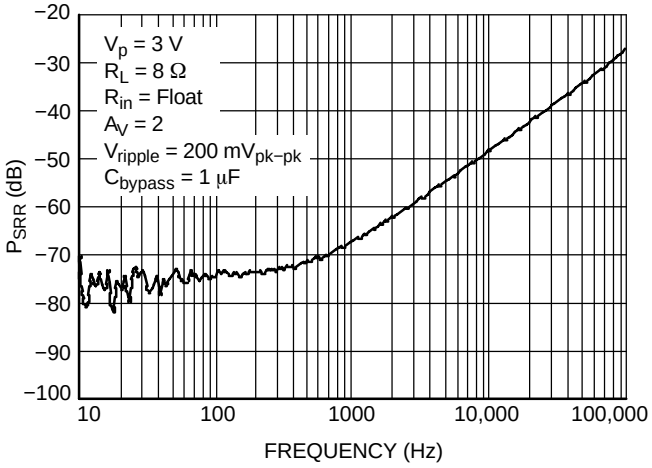


Figure 17. P_{SRR} @ V_p = 3 V

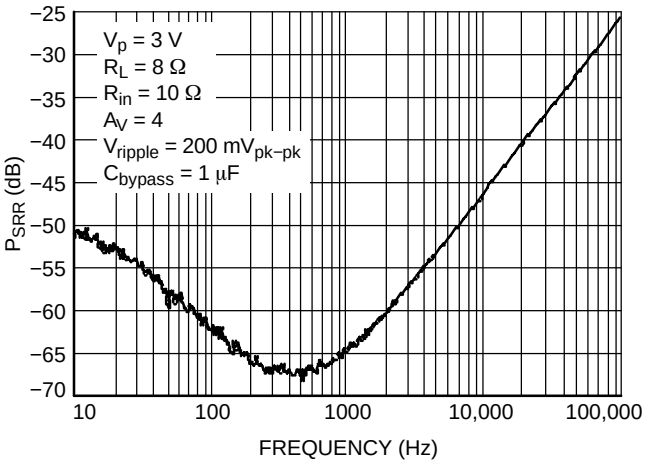


Figure 18. P_{SRR} @ V_p = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

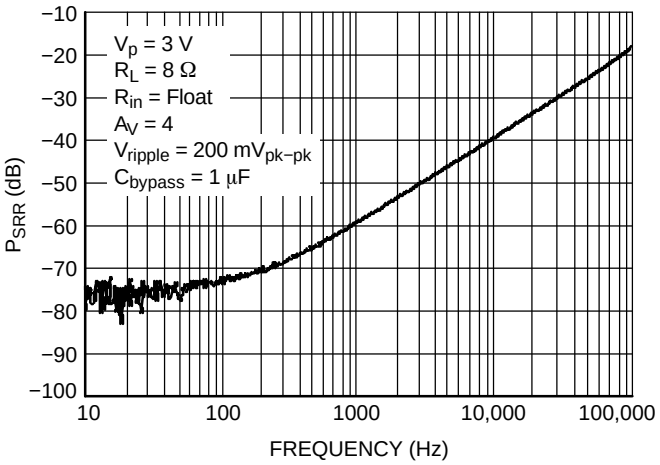


Figure 19. P_{SRR} @ V_p = 3 V

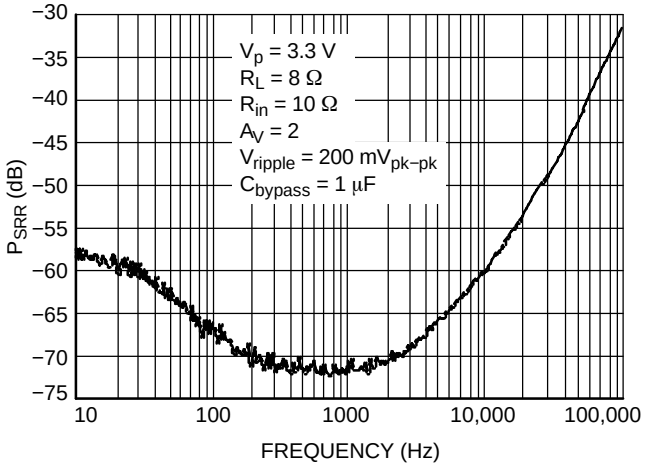


Figure 20. P_{SRR} @ V_p = 3.3 V

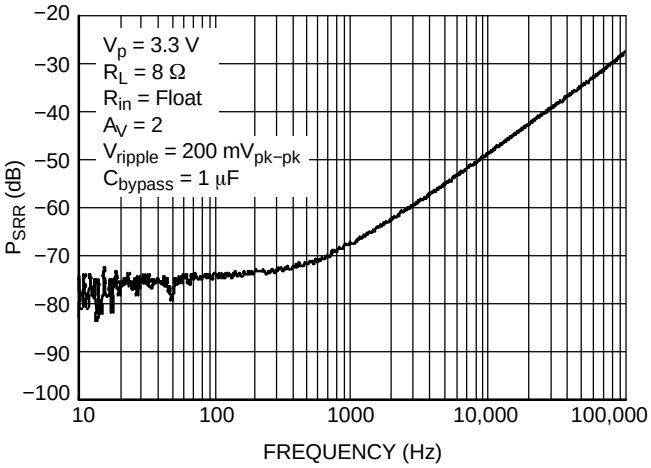


Figure 21. P_{SRR} @ V_p = 3.3 V

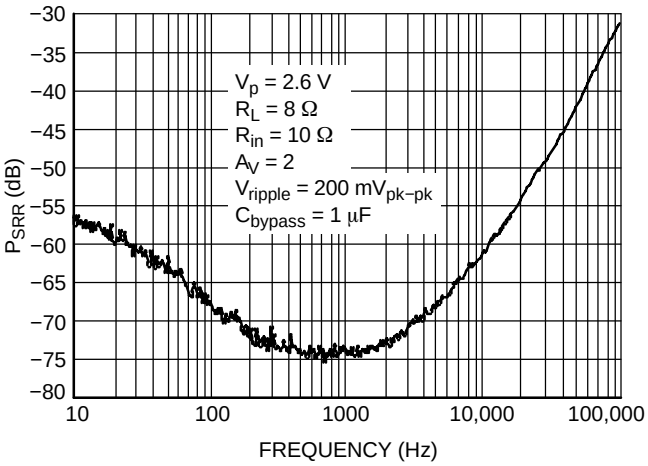


Figure 22. P_{SRR} @ V_p = 2.6 V

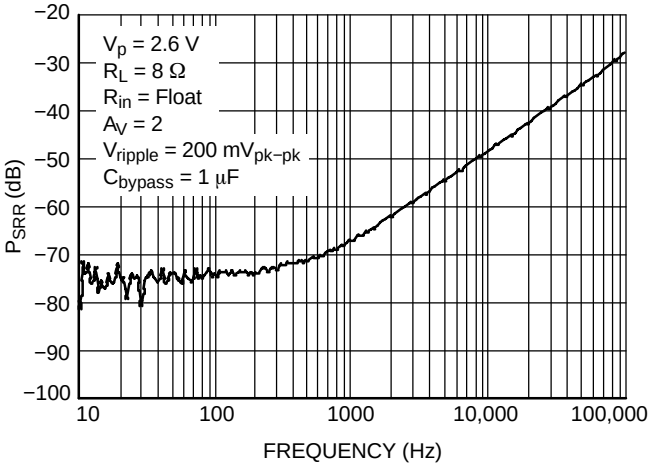


Figure 23. P_{SRR} @ V_p = 2.6 V

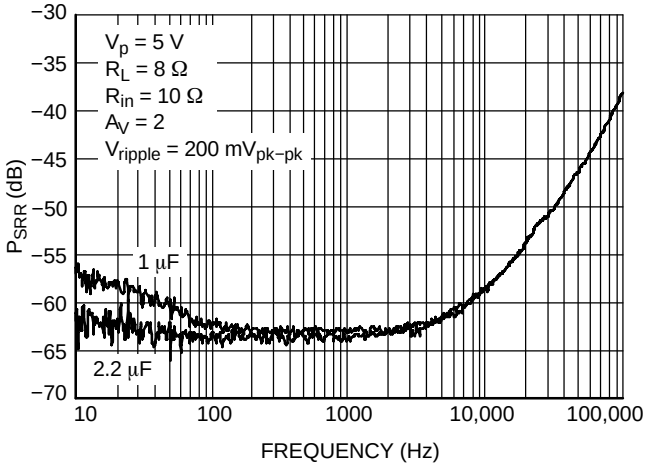


Figure 24. P_{SRR} versus C_{bypass} @ V_p = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

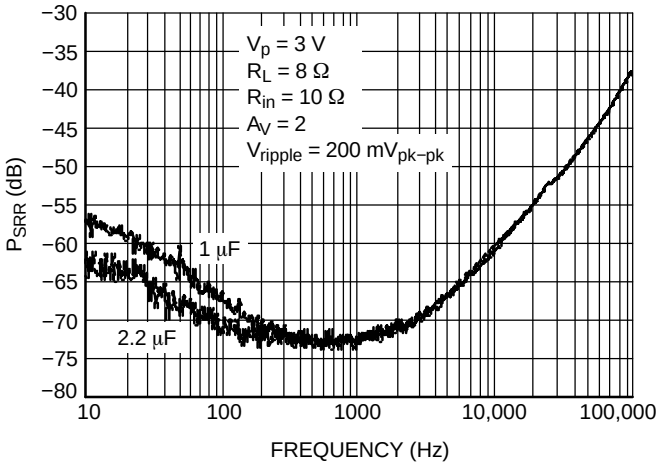


Figure 25. P_{SRR} versus C_{bypass} @ V_p = 3 V

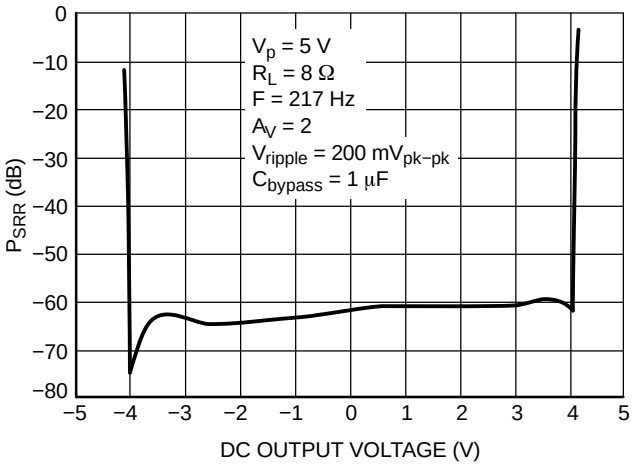


Figure 26. P_{SRR} @ DC Output Voltage

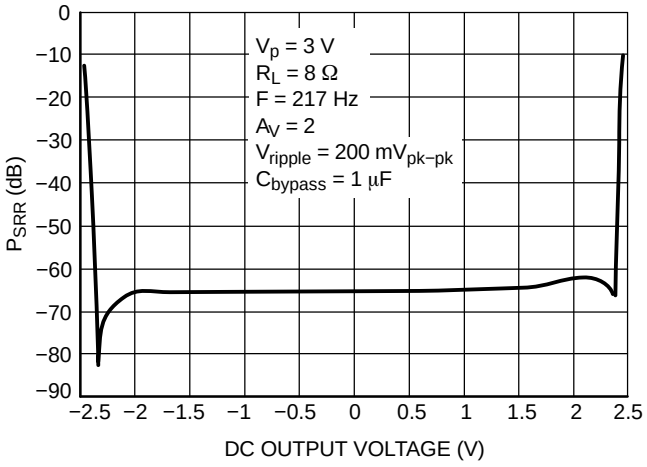


Figure 27. P_{SRR} @ DC Output Voltage

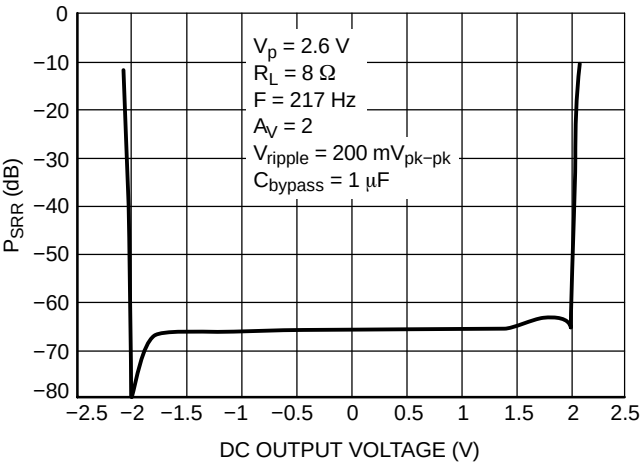


Figure 28. P_{SRR} @ DC Output Voltage

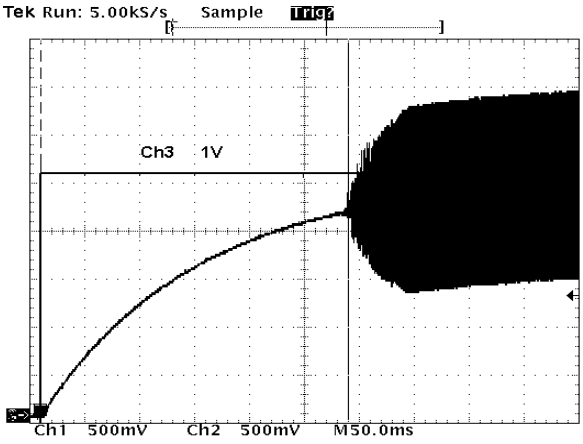


Figure 29. Turning On Time − V_p = 5 V

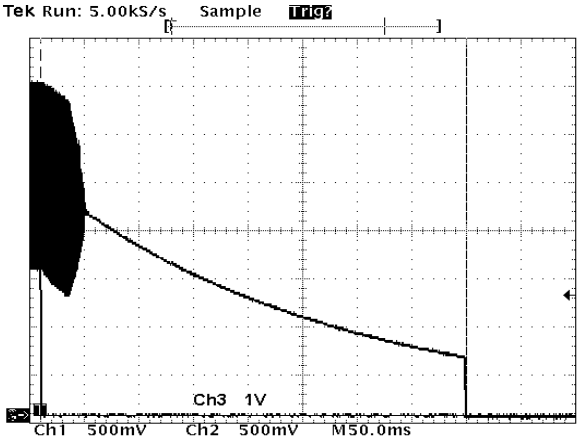


Figure 30. Turning Off Time − V_p = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

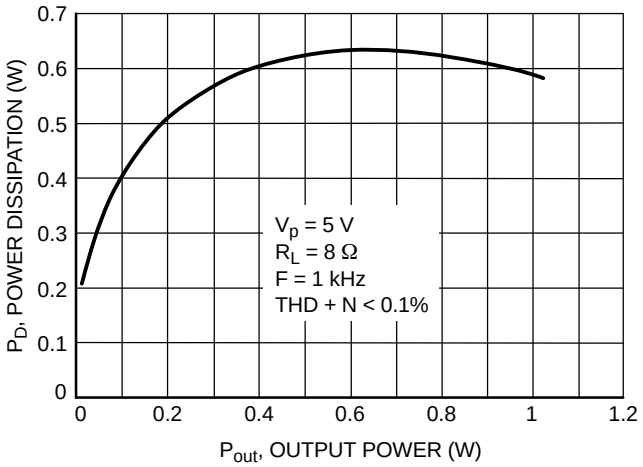


Figure 31. Power Dissipation versus Output Power

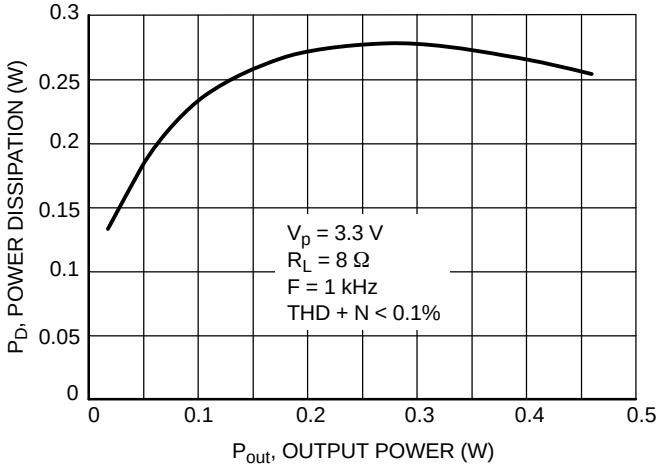


Figure 32. Power Dissipation versus Output Power

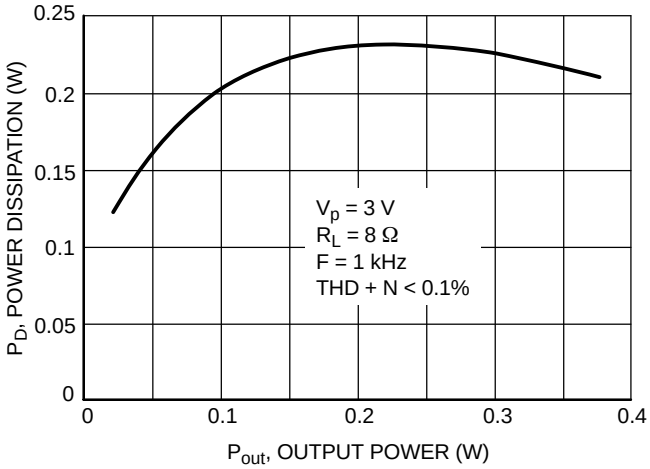


Figure 33. Power Dissipation versus Output Power

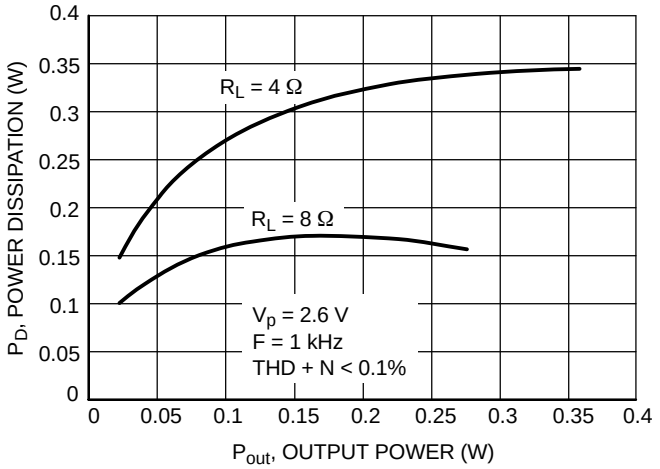


Figure 34. Power Dissipation versus Output Power

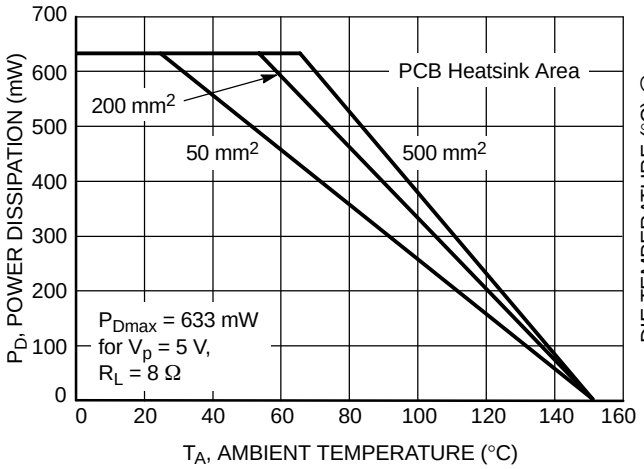


Figure 35. Power Derating − 9−Pin Flip−Chip CSP

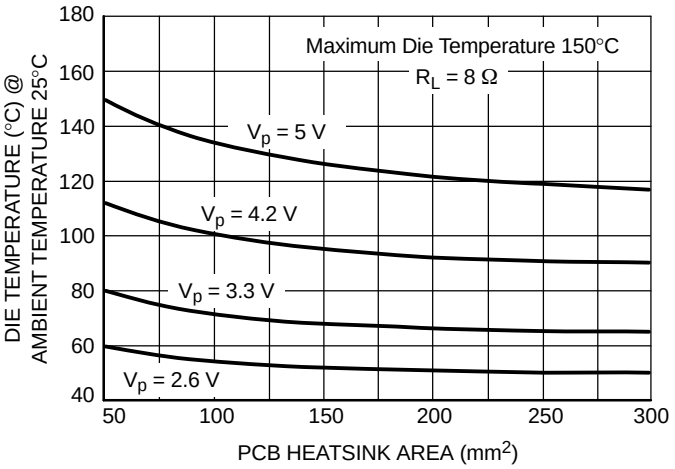


Figure 36. Maximum Die Temperature versus PCB Heatsink Area

APPLICATION INFORMATION

Detailed Description

The NCP2890 audio amplifier can operate under 2.6 V until 5.5 V power supply. It delivers 320 mW rms output power to 4.0 Ω load (V_p = 2.6 V) and 1.0 W rms output power to 8.0 Ω load (V_p = 5.0 V).

The structure of the NCP2890 is basically composed of two identical internal power amplifiers; the first one is externally configurable with gain−setting resistors R_{in} and R_f (the closed−loop gain is fixed by the ratios of these resistors) and the second is internally fixed in an inverting unity−gain configuration by two resistors of 20 kΩ. So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

Internal Power Amplifier

The output PMOS and NMOS transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors does not exceed 0.6 Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn−On and Turn−Off Transitions

A cycle with a turn−on and turn−off transition is illustrated with plots that show both single ended signals on the previous page.

In order to eliminate “pop and click” noises during transitions, output power in the load must be slowly established or cut. When logic high is applied to the shutdown pin, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the gain is established slowly (50 ms). This way to turn−on the device is optimized in terms of rejection of “pop and click” noises.

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. During the shutdown mode, amplifier outputs are connected to the ground.

When a shutdown low level is applied, it takes 350 ms before the DC output level is tied to Ground. However, as shown on Figure 30, the turn off time of the audio signal is 40 ms.

A theoretical value of turn−on time at 25°C is given by the following formula.

C_{by}: bypass capacitor

R: internal 300 k resistor with a 25% accuracy

T_{on} = 0.95 * R * C_{by} (285 ms with C_{by} = 1 μF)

If a faster turn on time is required then a lower bypass capacitor can be used. The other option is to use NCP2892 which offers 100 ms with 1 μF bypass capacitor.

Shutdown Function

The device enters shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 100 nA.

Current Limit Circuit

The maximum output power of the circuit (Porms = 1.0 W, V_p = 5.0 V, R_L = 8.0 Ω) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short−circuit occurs, the current limit in the load is fixed to 800 mA. The current in the four output MOS transistors are real−time controlled, and when one current exceeds 800 mA, the gate voltage of the MOS transistor is clipped and no more current can be delivered.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases fewer than 140°C.

The NCP2890 is unity−gain stable and requires no external components besides gain−setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

The first amplifier is externally configurable (R_f and R_{in}), while the second is fixed in an inverting unity gain configuration.

The differential−ended amplifier presents two major advantages:

- The possible output power is four times larger (the output swing is doubled) as compared to a single−ended amplifier under the same conditions.
- Output pins (OUTA and OUTB) are biased at the same potential $V_p/2$, this eliminates the need for an output coupling capacitor required with a single−ended amplifier configuration.

The differential closed loop−gain of the amplifier is given by $A_{vd} = 2 * \frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$.

Output power delivered to the load is given by $P_{orms} = \frac{(Vopeak)^2}{2 * R_L}$ (Vopeak is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA $I_{opeak} = \frac{V_{opeak}}{R_L}$.

Gain−Setting Resistor Selection (R_{in} and R_f)

R_{in} and R_f set the closed−loop gain of the amplifier.

In order to optimize device and system performance, the NCP2890 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor (R_{in}) value of 22 kΩ is realistic in most of applications, and doesn't require the use of a too large capacitor C_{in}.

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in}, the cut−off frequency is given by $fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}$.

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage (V_p/2) and can increase the turn−on pops.

An input capacitor value between 0.1 μ and 0.39 μF performs well in many applications (With R_{in} = 22 KΩ).

Bypass Capacitor Selection (Cby)

The bypass capacitor Cby provides half−supply filtering and determines how fast the NCP2890 turns on.

This capacitor is a critical component to minimize the turn−on pop. A 1.0 μF bypass capacitor value (C_{in} = < 0.39 μF) should produce clickless and popless shutdown transitions. The amplifier is still functional with a 0.1 μF capacitor value but is more susceptible to "pop and click" noises.

Thus, a 1.0 μF bypassing capacitor is recommended.

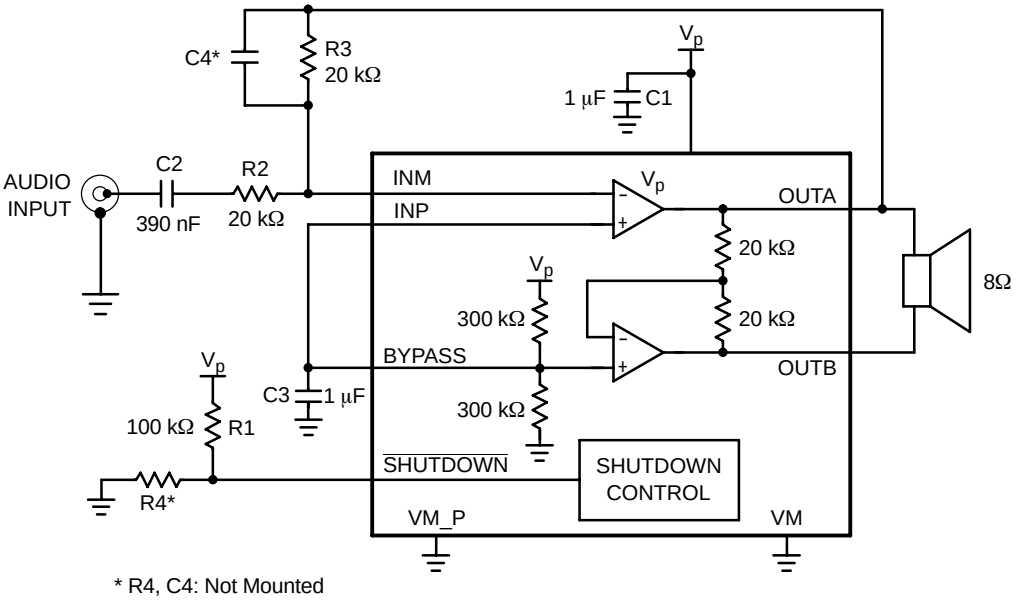
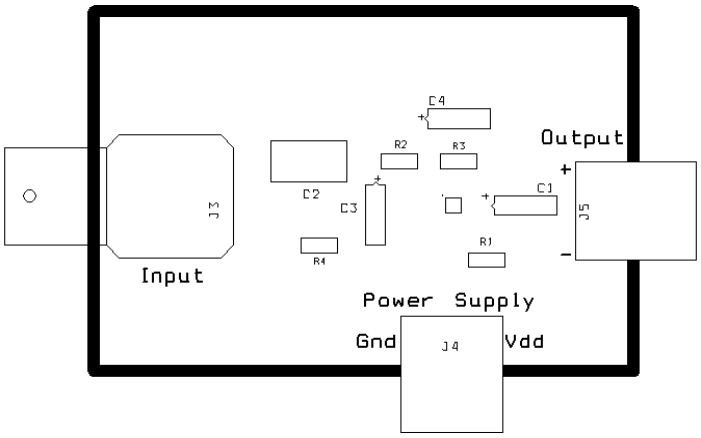
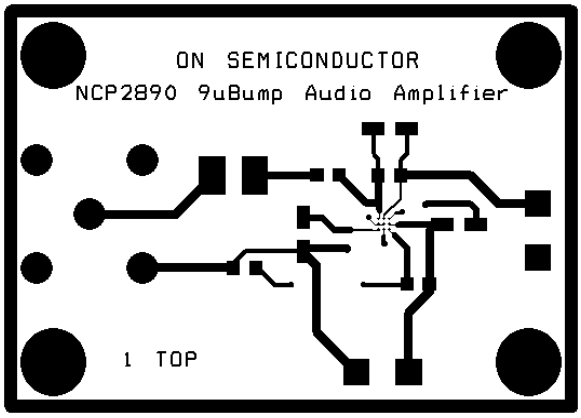


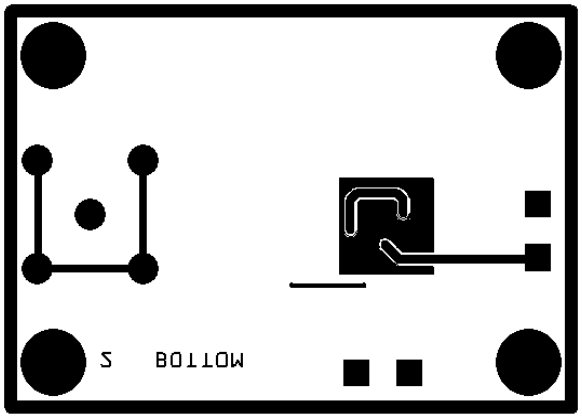
Figure 37. Schematic of the Demonstration Board of the 9−Pin Flip−Chip CSP Device



Silkscreen Layer



Top Layer



Bottom Layer

Figure 38. Demonstration Board for 9−Pin Flip−Chip CSP Device − PCB Layers

BILL OF MATERIAL

Item	Part Description	Ref.	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP2890 Audio Amplifier	–	–	ON Semiconductor	NCP2890
2	SMD Resistor 100 KΩ	R1	0805	Vishay−Draloric	D12CRCW Series
3	SMD Resistor 20 KΩ	R2, R3	0805	Vishay−Draloric	CRCW0805 Series
4	Ceramic Capacitor 1.0 μF 16 V X7R	C1	1206	Murata	GRM42−6X7R105K16
5	Ceramic Capacitor 390 nF 50 V Z5U	C2	1812	Kemet	C1812C394M5UAC
6	Ceramic Capacitor 1.0 μF 16 V X7R	C3	1206	Murata	GRM42−6X7R105K16
7	Not Mounted	R4, C4	–	–	–
8	BNC Connector	J3	–	Telegartner	JO1001A1948
9	I/O Connector. It can be plugged by BLZ5.08/2 (Weidmüller Reference)	J4, J5	–	Weidmüller	SL5.08/2/90B

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP2890AFCT2	MAG	9−Pin Flip−Chip CSP	3000/Tape and Reel
NCP2890AFCT2G	MAH	9−Pin Flip−Chip CSP (Pb−Free)	3000/Tape and Reel
NCP2890DMR2	MAB	Micro8	4000/Tape and Reel
NCP2890DMR2G	MAB	Micro8 (Pb−Free)	4000/Tape and Reel
NCV2890DMR2G	MBZ	Micro8 (Pb−Free)	4000/Tape and Reel

NOTE: This product is offered with either eutectic (SnPb−tin/lead) or lead−free solder bumps (G suffix) depending on the PCB assembly process. The NCP2890AFCT2G version requires a lead−free solder paste and should not be used with a SnPb solder paste.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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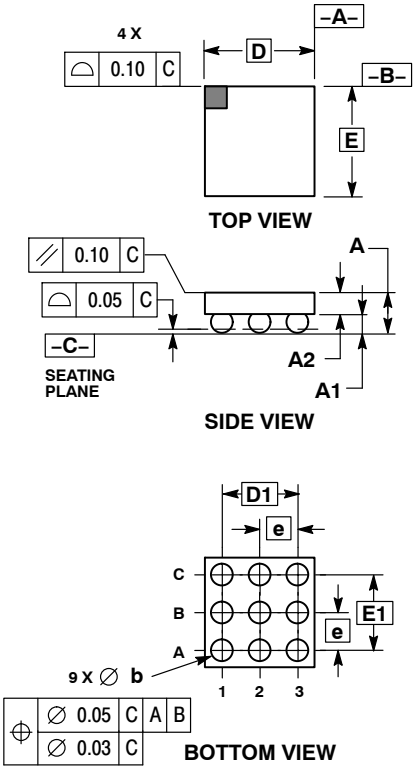
9 PIN FLIP−CHIP
CASE 499E−01
ISSUE A

DATE 30 JUN 2004

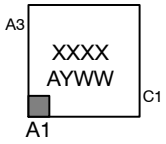
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*



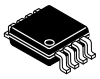
XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON12066D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**9 PIN FLIP−CHIP, 1.45 X 1.45 MM**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

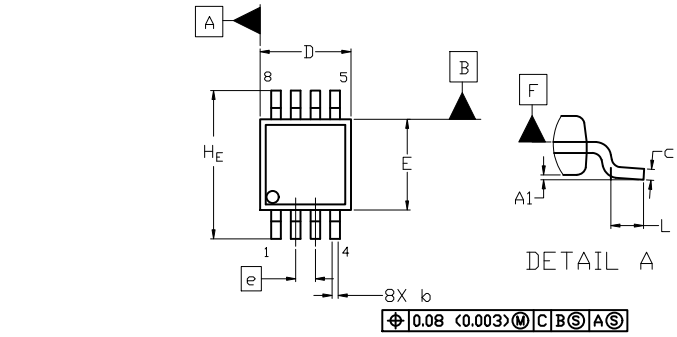
ON Semiconductor®

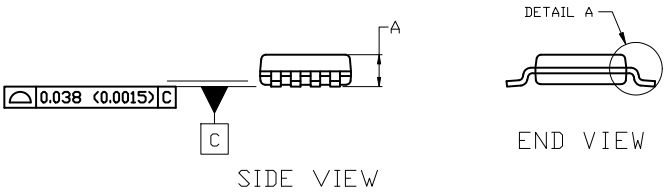


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

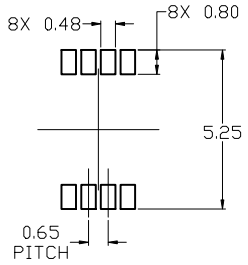
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

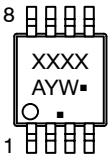


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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