Multi-rate Telecom Backplane SERDES for 2.5 Gbit/s Interconnect

FEATURES

- High performance backplane interface and cross-connect for 2.5G line cards in SONET/SDH systems.
- Provides one low-speed parallel TelecomBus interface operating at 32 bits x 77.76 MHz.
- Provides three high-speed multi-rate serial backplane interfaces.
- Supports CLOS and memory-based switch fabric systems.
- Supports linear, UPSR, and BLSR protection strategies.

SWITCHING CAPACITY

- Implements a 10G memory switch fabric with STS-1/AU-3 switching granularity in a single device.
- Supports non-blocking anycast switching between any of the serial or parallel interfaces.
- Provides two pages of connection memory with software and hardware controlled hitless page swaps at frame boundaries.
- Provides integrated delay management that allows for arbitrary SONET/SDH frame alignments on each ingress serial link.

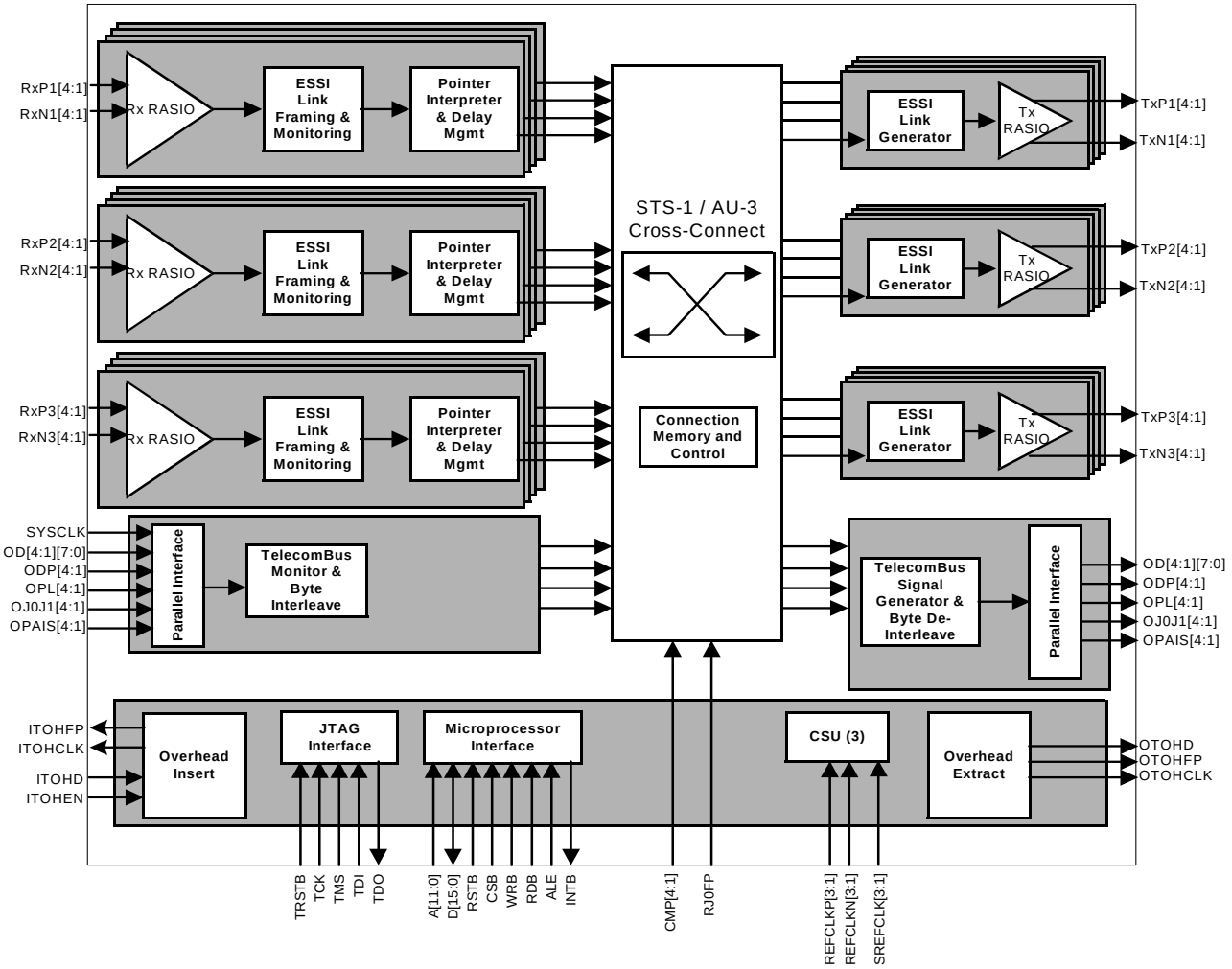
SERIAL PORT FUNCTIONS

- Supports three RASIO 3G high-speed serial backplane interfaces for interfacing with SONET/SDH cross-connects, framers, mappers, and other TBS™ 2488 devices.
- Each high-speed serial backplane interface is capable of independent operation at 4x622 Mbit/s scrambled NRZ SONET/SDH, 4x777 Mbit/s Serial TelecomBus, or 1x2488 Mbit/s scrambled NRZ SONET/SDH.
- High-speed serial RASIO compatible with CML, LVDS, and LVPECL.
- Supports nibble and di-bit slicing on 622 Mbit/s links for sliced switching architectures.

PARALLEL PORT FUNCTIONS

- Supports one 32-bit or four 8-bit 77.76 MHz TelecomBus interfaces to interface with parallel TelecomBus framers and mappers.
- Integrated pointer interpreter reduces complexity of external framers and mappers by asserting payload, J0, and J1 indications on the outgoing TelecomBus interface.
- Allows insertion and extraction of TOH bytes through a dedicated low speed serial interface.

BLOCK DIAGRAM



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- Provides Bit Error Rate (BER) monitoring for all paths received on the TelecomBus interface.
- Detects signal degrade (SD-P) and signal fail (SF-P) threshold crossing alarms based on received B3 errors on the TelecomBus interface.

ESSI FUNCTIONS

- Automatically frames to the incoming links based on standard A1/A2 framing.
- Provides in-service link verification via bit interleaved parity (BIP-8) of the B1 byte.
- Optionally generates B1 byte on egress flows.
- Provides out of frame alignment status information for each ingress port.
- Provides per-link SONET-framed and unframed PRBS-23 generation and monitoring for off-line link verification.
- Supports frame synchronization using ESSI smart framing or a global frame pulse input signal.
- Compensates for in frame boundary arrival times between serial interfaces using FIFOs and device level software configurable delay registers.

GENERAL

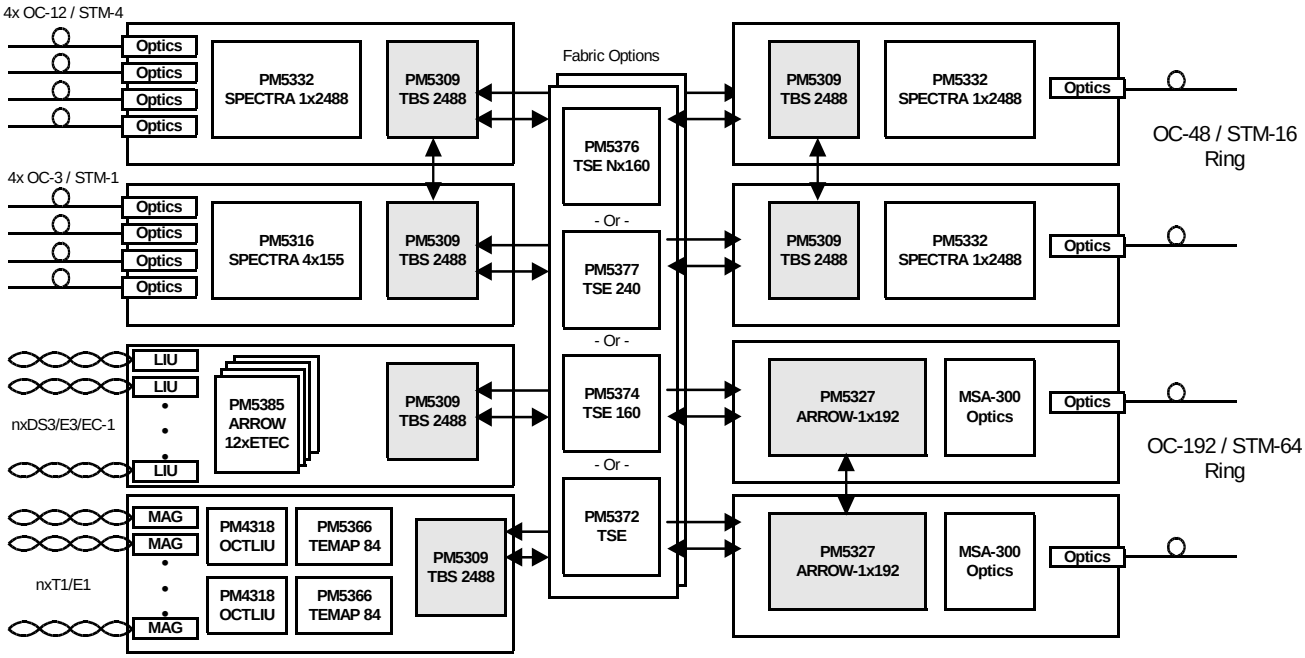
- Low power 1.2 V CMOS core with 2.5 V or 3.3 V CMOS/TTL selectable digital I/O.
- Generic 16-bit microprocessor bus interface and full suite of interrupts for configuration, control, and status monitoring.
- Standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board testing.

APPLICATIONS

- Multi-service Provisioning Platforms.
- SONET/SDH Digital Cross-connects.
- SONET/SDH Add/Drop and Terminal Multiplexers.

TYPICAL APPLICATIONS

STS-1 BASED CROSS-CONNECTS AND MSPP'S



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