

FAST CMOS 16-BIT ID REGISTERED/LATCHED TRANSCEIVER WITH PARITY

IDT54/74FCT162511AT/CT

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical tsk(o) (Output Skew) < 250ps, clocked mode
- Low input and output leakage ≤1µA (max)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 5V ±10%
- Balanced Output Drivers:
 - ±24mA (industrial)
 - ±16mA (military)
- · Series current limiting resistors
- · Generate/Check, Check/Check modes
- · Open drain parity error allows wire-OR
- Available in the following packages:
 - Industrial: SSOP, TSSOP
 - Military: CERPACK

DESCRIPTION:

The FCT162511T 16-bit registered/latched transceiver with parity is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The device has a parity generator/ checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. Separate error flags exits for each direction with a single error flag indicating an error for either byte in the A-to-B direction. The parity error flags are open drain outputs which can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. The parity error flags are enabled by the OExx control pins allowing the designer to disable the error flag during combinational transitions.

The control pins LEAB, CLKAB, and OEAB control operation in the A-to-B direction while LEBA, CLKBA, and OEBA control the B-to-A direction. GEN/ CHK is only for the selection of A-to-B operation. The B-to-A direction is always inchecking mode. The ODD/EVEN selectis common between the two directions. Except for the ODD/EVEN control, independent operation can be achieved between the two directions by using the corresponding control lines.

I FAB CLKAB OEAB Data Parity, data B0-15 16 18 PB1.2 Parity Latch/ **GEN/CHK** Register Byte 2 Parity PERB Generator/ A0-15 -(Open Drain) Checker PA1,2 ODD/EVEN LEBA **CLKBA** Parity, Data Parity, data 18 18 Latch/ OEBA Register Byte Parity PERA Checking (Open Drain)

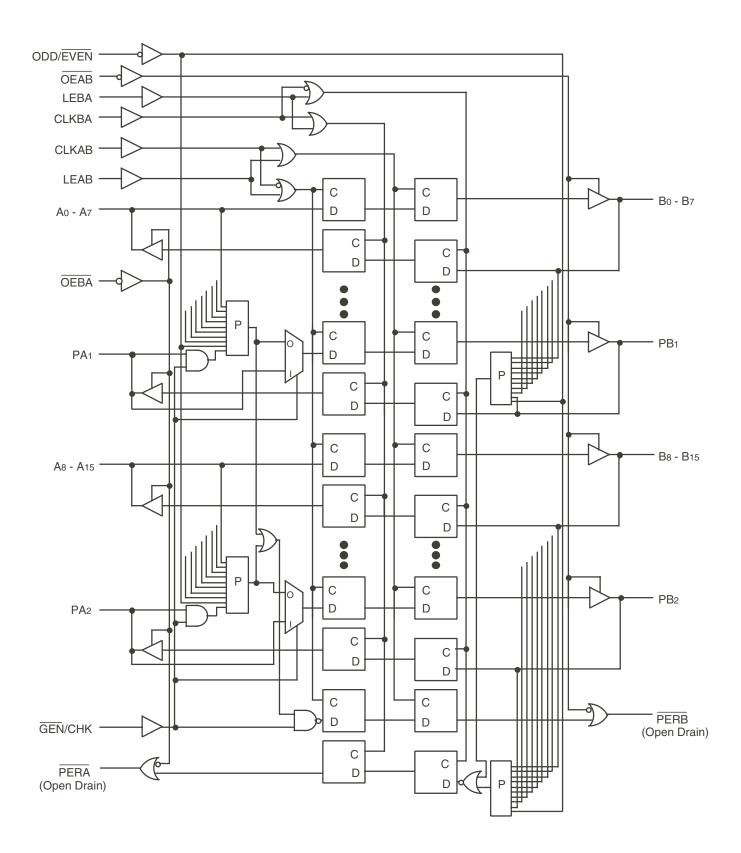
FUNCTIONAL BLOCK DIAGRAM

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MILITARY AND INDUSTRIAL TEMPERATURE RANGES

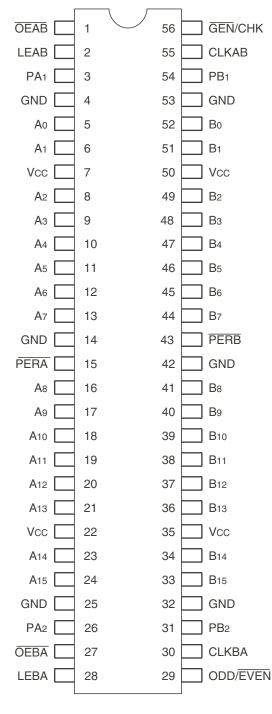
SEPTEMBER 2009

BLOCK DIAGRAM



MILITARY AND INDUSTRIAL TEMPERATURE RANGES

PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	–0.5 to 7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
Tstg	Storage Temperature	-65 to +150	°C
Ιουτ	DC Output Current	-60 to +120	mA

NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. All device terminals except FCT162XXX Output and I/O terminals.

3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
Ci/o	I/O Capacitance	Vout = 0V	3.5	8	pF
Co	Open Drain Capacitance	Vout = 0V	3.5	6	pF

PIN DESCRIPTION

Pin Names	Description
ŌĒĀB	A-to-B Output Enable Input (Active LOW)
ŌĒBĀ	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Вх	B-to-A Data Inputs or A-to-B 3-State Outputs
PERA	Parity Error (Open Drain) on A Outputs
PERB	Parity Error (Open Drain) on B Outputs
PAx ⁽¹⁾	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
ODD/EVEN	Parity Mode Selection Input
GEN/CHK	A to B Port Generate or Check Mode Input

NOTE:

 The PAx pin input is internally disabled during parity generation. This means that when generating parity in the A to B direction there is no need to add a pull up resistor to guarantee state. The pin will still function properly as the parity output for the B to A direction.

FUNCTION TABLE^(1, 4)

	Inputs							
OEAB	LEAB	CLKAB	Ах	Вх				
Н	Х	Х	Х	Z				
L	Н	Х	L	L				
L	Н	Х	Н	Н				
L	L	↑	L	L				
L	L	↑	Н	Н				
L	L L		Х	B ⁽²⁾				
L	L	Н	Х	B ⁽³⁾				

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
 Output level before the indicated steady-state input conditions were established,
- provided that CLKAB was HIGH before LEAB went LOW.
- 4. H = HIGH Voltage Level
 - L = LOW Voltage Level
 - X = Don't Care
 - Z = High-impedance
 - ↑ = LOW-to-HIGH Transition

FUNCTION TABLE (PARITY CHECKING) ^(1, 2, 3, 4)

A0 – A7 and PA1 ⁽⁵⁾		
Number of inputs that are high	ODD/EVEN	PERB
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	Н	H ⁽⁶⁾
0, 2, 4, 6 or 8	L	H ⁽⁶⁾
0, 2, 4, 6 or 8	Н	L

NOTES:

- 1. Conditions shown are for $\overline{\text{GEN}}/\text{CHK} = \text{H}$, $\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$.
- A-to-B parity checking is shown. B-to-A parity checking is similar but uses OEBA = L, OEAB = H and errors will be indicated on PERA.
- In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors (PB1 = PA1).
- 4. The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
- 5. Conditions shown are for the byte A0-A7 and PA1. The byte A8-A15 and PA2 is similiar.
- 6. The parity error flag PERB is a combined flag for both bytes A0–A7 and A8–A15. If a parity error occurs on either byte PERB will go low. PERB is an open drain output which must be externally pulled up to achieve a logic HIGH.

FUNCTION TABLE (PARITY GENERATION) (1, 2, 3, 4, 5)

A0 – A7 Number of inputs that are high	ODD/EVEN	PB1
1, 3, 5 or 7	L	Н
1, 3, 5 or 7	Н	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	Н	Н

NOTES:

- 1. Conditions shown are for $\overline{\text{GEN}}/\text{CHK} = L$, $\overline{\text{OEAB}} = L$, $\overline{\text{OEBA}} = H$.
- A-to-B parity checking is shown. B-to-A is capable of parity checking while A-to-B is performing generation. B-to-A will not generate parity.
- The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
- Conditions shown are for the byte A–A7. The byte A8–A15 is similiar but will output the parity on PB2.
- 5. The error flag PERB will remain in a high state during parity generation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = 5.0V $\pm 10\%$; Military: TA = -55° C to $+125^{\circ}$ C, VCC = 5.0V $\pm 10\%$

Symbol	Parameter	Test Condit	ions ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Unit
Vih	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	_	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		_	—	0.8	V
Іін	Input HIGH Current (Input pins) ⁽⁵⁾	Vcc = Max. VI = Vcc		_	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			_	—	±1	
lıL	Input LOW Current (Input pins) ⁽⁵⁾		VI = GND	_	—	±1	
	Input LOW Current (I/O pins) ⁽⁵⁾			_	_	±1	
Іоzн	High Impedance Output Current	Vcc = Max.	Vo = 2.7V	_	—	±1	μA
Iozl	(3-State Output pins) ⁽⁵⁾		Vo = 0.5V	_	—	±1	
Vik	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		Ι	-0.7	-1.2	V
los	Short Circuit Current	Vcc = Max., Vo = GND ⁽³⁾		-80	-140	-250	mA
Vн	Input Hysteresis	_		_	100	—	mV
Іссь Іссн Іссz	Quiescent Power Supply Current	Vcc = Max. Vin = GND or Vcc		_	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
IODL	Output LOW	(I/O pins)	VCC = 5V, VIN = VIH or VIL, VO = $1.5V^{(3)}$	3)	60	115	200	mA
	Current	(Open Drain)			_	250	_	mA
Iodh	Output HIGH Current		VCC = 5V, VIN = VIH or VIL, VO = $1.5V^{(3)}$	3)	-60	-115	-200	mA
IOFF	Output Power Off Leakage	Current	$Vcc = 0, Vo \le 5.5V$			—	±1	μA
	(Open Drain) ⁽⁵⁾							
Vон	Output HIGH Voltage (I/O	pins)	Vcc = Min.	Iон = –16mA MIL	2.4	3.3	—	V
			VIN = VIH or VIL	Iон = -24mA IND				
Vol	OutputLOW	(I/O pins)	Vcc = Min.	IOL = 16mA MIL	-	0.3	0.55	V
	Voltage		VIN = VIH or VIL	Iol = 24mA IND				
		(Open Drain)		Iol = 48mA MIL	—	0.3	0.55	V
				Iol = 64mA IND				

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at Vcc = 5.0V, +25°C ambient.

3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

4. Duration of the condition can not exceed one second.

5. The test limit for this parameter is $\pm 5\mu A$ at TA = $-55^{\circ}C$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Tes	Test Conditions ⁽¹⁾			Max.	Unit
Δlcc	Quiescent Power Supply Current	Vcc = Max.	Vcc = Max. All other Input Pins		0.5	1.5	mA
	TTL Inputs HIGH	$VIN = 3.4V^{(3)}$	Parity Input Pins (PAx,	PBx) —	1	2.5	
ICCD	Dynamic Power Supply Current ⁽⁴⁾	Vcc = Max. Outputs Open OEAB = GND, OEBA = One Input Togging 50% Duty Cycle	VIN = VCC VIN = GND VCC	_	75	120	μΑ/ MHz
IC	Total Power Supply Current ⁽⁶⁾	Vcc = Max. Outputs Open fcP = 10MHz (CLKAB) 50% Duty Cycle OEAB = GND, OEBA =	VIN = VCC VIN = GND VCC	_	0.8	1.7	mA
		LEAB = GND One Bit Toggling fi = 5MHz 50% Duty Cycle	VIN = 3.4V VIN = GND	-	1.3	3.2	
		Vcc = Max. Outputs Open fcP = 10MHz (CLKAB) 50% Duty Cycle OEAB = GND, OEBA =	VIN = VCC VIN = GND VCC	-	3.8	6.5 ⁽⁵⁾	
		LEAB = GND Eighteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	VIN = 3.4V VIN = GND	-	9	21.8 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at Vcc = 5.0V, +25°C ambient.

- 3. Per TTL driven input (VIN = 3.4V). All other inputs at Vcc or GND.
- 4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- 5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.

6. IC = IQUIESCENT + INPUTS + IDYNAMIC

- IC = ICC + Δ ICC DHNT + ICCD (fCPNCP/2 + fiNi)
- Icc = Quiescent Current (IccL, IccH and Iccz)
- Δ Icc = Power Supply Current for a TTL High Input (VIN = 3.4V)
- DH = Duty Cycle for TTL Inputs High
- NT = Number of TTL Inputs at DH
- Icco = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
- fcp = Clock Frequency for Register Devices (Zero for Non-Register Devices)
- NCP = Number of Clock Inputs at fCP
- fi = Input Frequency
- Ni = Number of Inputs at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (PROPAGATION DELAYS)

				FCT162511AT				FCT16	2511CT		
			In	d.	M	lil.	In	d.	М	il.	
Symbol	Parameter	Condition ⁽¹⁾	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Unit
tPLH .	Propagation Delay, PAx to PBx	CL = 50pF	1.5	5	1.5	5.3	1.5	4.2	1.5	4.5	ns
t PHL	Ax to Bx or Bx to Ax, PBx to PAx	RL = 500Ω									
tplh tphl	Propagation Delay GEN/CHK LOW Ax to PBx		1.5	7.5	1.5	8	1.5	6.5	1.5	6.8	ns
tPLH ⁽³⁾	Propagation Delay	1	1.5	9	1.5	9	1.5	7.5	1.5	7.8	ns
t PHL	Ax to PERB, PAx to PERB		1.5	8	1.5	8	1.5	6.5	1.5	6.8	ns
tPLH ⁽³⁾	Propagation Delay	1	1.5	9	1.5	9	1.5	7.5	1.5	7.8	ns
t PHL	Bx to PERA, PBx to PERA		1.5	8	1.5	8	1.5	6.5	1.5	6.8	ns
tPLH .	Propagation Delay	1									
t PHL	LEBA to Ax and PAx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
	LEAB to Bx and PBx										
tPLH ⁽³⁾	Propagation Delay	1	1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t PHL	LEBA to PERA, LEAB to PERB		1.5	6	1.5	6	1.5	5	1.5	5.3	ns
tPLH .	Propagation Delay	1									
t PHL	CLKBA to Ax and PAx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
	CLKAB to Bx and PBx										
tPLH ⁽³⁾	Propagation Delay		1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t PHL	CLKBA to PERA		1.5	6	1.5	6	1.5	5	1.5	5.3	ns
	CLKAB to PERB		1.0	0	1.0	0	1.0	5	1.0	0.5	115
tрzн	Output Enable Time										
tPZL	OEBA to Ax and PAx		1.5	6	1.5	6.5	1.5	5.6	1.5	5.8	ns
	OEAB to Bx and PBx										
tPHZ	Output Disable Time										
tPLZ	OEBA to Ax and PAx		1.5	5.6	1.5	6	1.5	5.2	1.5	5.5	ns
	OEAB to Bx and PBx										
tPLZ ⁽³⁾	Parity ERROR Enable		1.5	6	1.5	6.3	1.5	6	1.5	6.3	ns
tPZL	OEBA to PERA, OEAB to PERB		1.5	6	1.5	6.3	1.5	6	1.5	6.3	ns
tPLH ⁽³⁾	ODD/EVEN to PERx		1.5	10	1.5	10	1.5	10	1.5	10	ns
t PHL		1	1.5	10	1.5	10	1.5	10	1.5	10	ns
tPLH	ODD/EVEN to PBx		1.5	10	1.5	10	1.5	10	1.5	10	ns
TPHL NOTES.											

NOTES:

1. See test circuits and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

3. On Open Drain Outputs tPLH is measured at VOUT = VOL + 0.3V.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (SET UP TIMES)

						FCT16	2511A	Т	F	CT162	511CT		
					In	Ind.		Mil.		Ind.		Mil.	
Symbol	Parameter	Test Con	ditions ^(1, 3)		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tsu	Set-up Time	GEN/CHK LOW	PBx valid	CL = 50pF	4	_	4	—	3	—	3.5	—	ns
	HIGH or LOW		PBx not valid	$RL = 500\Omega$	3	_	3	_	3	_	3	_	ns
	Ax to CLKAB	GEN/CHK HIGH	PERB valid		4	_	4	_	3	_	3	_	ns
			PERB not valid		3		3	_	3	_	3	_	ns
tsu	Set-up Time	GEN/CHK HIGH	PERB valid		4	_	4	_	3	_	3	_	ns
	PAx to CLKAB		PERB not valid		3	_	3	_	3	_	3	_	ns
tsu	Set-up Time		PERA valid		4	_	4	_	3		3	_	ns
	Bx to CLKBA,		PERA not valid		3	-	4	—	3	-	3	—	ns
	PBx to CLKBA												
tsu	Set-up Time	CLKAB LOW	PBx valid		3.5	_	3.5	_	3	_	3	_	ns
	Ax to LEAB	GEN/CHK LOW	PBx not valid		3	_	3	_	3	_	3	_	ns
		CLKAB LOW	PERB valid		3.5	_	3.5	_	3		3	_	ns
		GEN/CHK HIGH	PERB not valid		3	_	3	_	3	_	3	—	ns
		CLKAB HIGH	PBx valid		3.5	_	3.5	_	3		3	_	ns
		GEN/CHK LOW	PBx not valid		3	_	3	_	3	—	3	—	ns
		CLKAB HIGH	PERB valid		3.5	_	3.5	_	3	_	3	_	ns
		GEN/CHK HIGH	PERB not valid		3	_	3	_	3	_	3	_	ns
tsu	Set-up Time	CLKAB LOW	PERB valid		3.5	_	3.5	_	3	_	3	_	ns
	PAx to LEAB	GEN/CHK HIGH	PERB not valid		3		3	_	3		3	_	ns
		CLKAB HIGH	PERB valid		3.5		3.5	_	3		3	_	ns
		GEN/CHK HIGH	PERB not valid		3		3	_	3		3		ns
tsu	Set-up Time	CLKBA LOW	PERA valid		3.5	_	3.5	_	3		3		ns
	Bx to LEBA		PERA not valid		3		3		3		3		ns
	PBx to LEBA	CLKBA HIGH	PERA valid		3.5		3.5		3		3		ns
			PERA not valid		3		3		3		3		ns
tsk(0)	Output Skew ⁽⁴⁾				-	0.5	—	0.5	-	0.5	—	0.5	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (HOLD TIMES)

			FCT162511AT			-	FCT162511CT				
			lr	Ind.		Ail.	Ind.		l. Mil.		
Symbol	Parameter	Condition ⁽¹⁾	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tH	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	CL= 50pF	1	_	1	—	1	—	1	—	ns
tH	Hold Time HIGH or LOW PAx to LEAB	RL = 500Ω	1		1	—	1	—	1	-	ns
tH	Hold Time HIGH or LOW PBx to LEBA]	1		1	—	1	—	1	—	ns
Ħ	Hold Time Ax to CLKAB, PAx to CLKAB]	1	_	1	—	0	—	0	—	ns
tH	Hold Time Bx to CLKBA, PBx to CLKBA]	1	_	1	—	0	—	0	-	ns
tw	LEAB or LEBA Pulse Width HIGH ⁽²⁾]	3	_	3	_	3	_	3	_	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽²⁾		3	_	3	-	3	_	3	_	ns

NOTES:

1. See test circuits and waveforms.

2. This parameter is guaranteed but not tested.

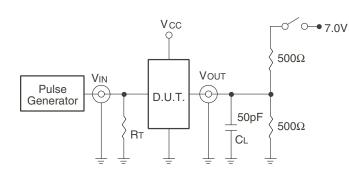
3. "Not valid" means the set-up time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A to B or B to A port respective to the indicated direction.

4. Skew between any two outputs of the same package, switching in the same direction, excluding PERx in clocked mode, and Pxx (parity bits) and PERx in transparent/ latched mode. This parameter is guaranteed by design.

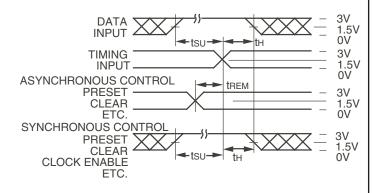
IDT54/74FCT162511AT/CT FASTCMOS16-BITREGISTERED/LATCHEDTRANSCEIVER

MILITARY AND INDUSTRIAL TEMPERATURE RANGES

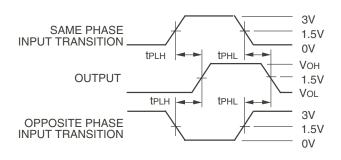
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

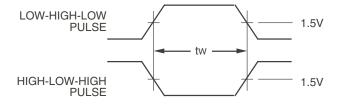
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

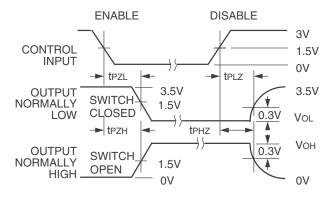
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

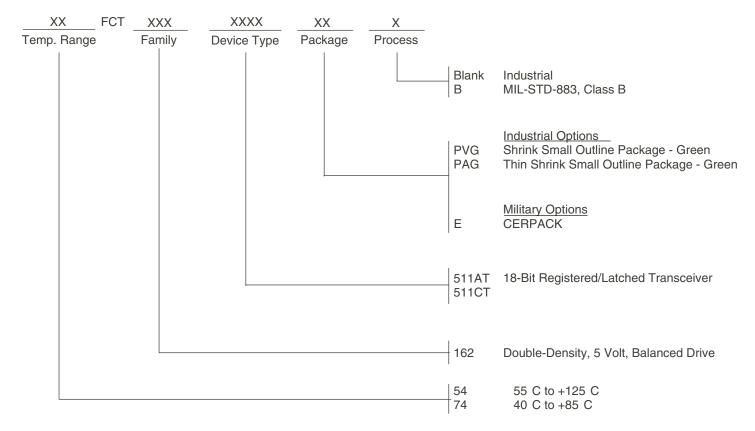




NOTES:

- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- 2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; tF \leq 2.5ns; tR \leq 2.5ns.

ORDERING INFORMATION



Datasheet Document History

09/06/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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