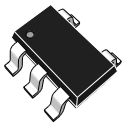
TSX711, TSX711A, TSX712

Datasheet

Low-power, precision, rail-to-rail, 2.7 MHz, 16 V CMOS operational amplifiers

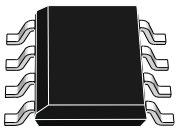
TSX711 and TSX711A



SOT23-5

TSX712

MiniSO8



SO8

Features

- Low input offset voltage: 200 µV max.
- Rail-to-rail input and output
- Low current consumption: 800 µA max.
- Gain bandwidth product: 2.7 MHz
- Low supply voltage: 2.7 - 16 V
- Unity gain stable
- Low input bias current: 50 pA max.
- High ESD tolerance: 4 kV HBM
- Extended temp. range: -40 °C to 125 °C
- Automotive qualification

Applications

- Battery-powered instrumentation
- Instrumentation amplifier
- Active filtering
- DAC buffer
- High-impedance sensor interface
- Current sensing (high and low side)

Maturity status link
TSX711, TSX711A, TSX712

Related products	
TSX7191, TSX7192	For higher speeds with similar precision
TSX561, TSX562	For low-power features
TSX631, TSX632	For micro-power features
TSX921, TSX922	For higher speeds

Description

The TSX711, TSX711A, and TSX712 series of operational amplifiers (op amps) offer high precision functioning with low input offset voltage down to a maximum of 200 µV at 25 °C. In addition, their rail-to-rail input and output functionality allow these products to be used on full range input and output without limitation. This is particularly useful for a low-voltage supply such as 2.7 V that the TSX71x is able to operate with.

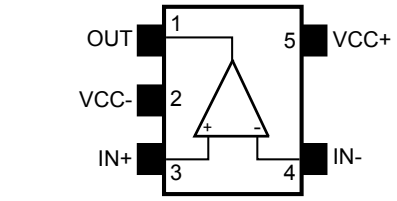
Thus, the TSX71x has the big advantage of offering a large span of supply voltages, ranging from 2.7 V to 16 V. They can be used in multiple applications with a unique reference.

Low input bias current performance makes the TSX71x perfect when used for signal conditioning in sensor interface applications. In addition, low-side and high-side current measurements can be easily made thanks to rail-to-rail functionality.

High ESD tolerance (4 kV HBM) and a wide temperature range are also good reasons to use the TSX71x in the automotive market segment.

1 Package pin connections

Figure 1. Pin connections (top view)



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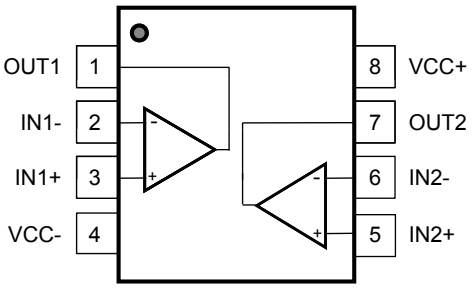


MiniSO8 and SO8

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		18	V
V_{id}	Differential input voltage (2)(3)		$\pm V_{CC}$	mV
V_{in}	Input voltage		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient (5)(6)	SOT23-5	250	°C/W
		MiniSO8	190	
		SO8	125	
T_j	Maximum junction temperature		150	°C
ESD	HBM: human body model (7)		4000	V
	MM: machine model (8)		100	
	CDM: charged device model (9)		1500	
	Latch-up immunity		200	mA

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. See Section 5.7 High values of input differential voltage for the precautions to follow when using the TSX711, TSX711A, and TSX712 with a high differential input voltage.*
3. *Input stage is protected against excessive differential voltage. Each input has a 1 kΩ resistor connected on the input, in series with the emitter of a PNP transistor with collector grounded. The base of the PNP is connected to the other input. This structure is present on both inputs. Therefore, in comparator mode, or when Vdiff becomes higher than a diode voltage (V_d ~ 0.7 V), the input with the highest voltage has a current of (V_{diff} - V_d) / 1 kΩ. The other input has a much lower input current as it is divided by the gain of the PNP. See Section 5.7 High values of input differential voltage for more details.*
4. *Input current must be limited by a resistor in series with the inputs.*
5. *R_{th} are typical values.*
6. *Short-circuits can cause excessive heating and destructive dissipation.*
7. *According to JEDEC standard JESD22-A114F.*
8. *According to JEDEC standard JESD22-A115A.*
9. *According to ANSI/ESD STM5.3.1*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{oper}	Operating free air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = 4 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 ° C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io} (TSX711, TSX712)	Input offset voltage	$V_{icm} = V_{CC}/2$			200	µV
		$T_{min} < T_{op} < 85$ °C			365	
		$T_{min} < T_{op} < 125$ °C			450	
V_{io} (TSX711A)		$V_{icm} = V_{CC}/2$			100	
		$T_{min} < T_{op} < 85$ °C			265	
		$T_{min} < T_{op} < 125$ °C			350	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		1		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current(1)	$V_{out} = V_{CC}/2$		1	50	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current(1)	$V_{out} = V_{CC}/2$		1	50	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR (TSX711, TSX711A)	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 4.1 V, $V_{out} = V_{CC}/2$	84	102		dB
		$T_{min} < T_{op} < T_{max}$	83			
		V_{icm} = -0.1 to 2 V, $V_{out} = V_{CC}/2$	100	122		
		$T_{min} < T_{op} < T_{max}$	94			
CMRR (TSX712)		V_{icm} = -0.1 to 4.1 V, $V_{out} = V_{CC}/2$	80	98		
		$T_{min} < T_{op} < T_{max}$	78			
		V_{icm} = -0.1 to 2 V, $V_{out} = V_{CC}/2$	91	103		
		$T_{min} < T_{op} < T_{max}$	86			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out} = 0.3 to 3.7 V	110	136		
		$T_{min} < T_{op} < T_{max}$	96			
		R_L = 10 kΩ, V_{out} = 0.2 to 3.8 V	110	140		
		$T_{min} < T_{op} < T_{max}$	96			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L = 2 kΩ to $V_{CC}/2$		28	50	mV
		$T_{min} < T_{op} < T_{max}$			60	
		R_L = 10 kΩ to $V_{CC}/2$		6	15	
		$T_{min} < T_{op} < T_{max}$			20	
V_{OL}	Low level output voltage	R_L = 2 kΩ to $V_{CC}/2$		23	50	mV
		$T_{min} < T_{op} < T_{max}$			60	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}/2		5	15	mV
		$T_{min} < T_{op} < T_{max}$			20	
I_{out} (TSX711, TSX711A)	I_{sink}	$V_{out} = V_{CC}$	35	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	I_{source}	V_{out} = 0 V	35	45		
		$T_{min} < T_{op} < T_{max}$	20			
I_{out} (TSX712)	I_{sink}	$V_{out} = V_{CC}$	25	37		
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	35	45		
		$T_{min} < T_{op} < T_{max}$	20			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}$/2		570	800	µA
		$T_{min} < T_{op} < T_{max}$			900	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		50		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 3 V_{PP}, 10 % to 90 %	0.6	0.85		V/µs
		$T_{min} < T_{op} < T_{max}$	0.5			
SRp	Positive slew rate	Av = 1, V_{out} = 3V_{PP}, 10 % to 90 %	1.0	1.4		
		$T_{min} < T_{op} < T_{max}$	0.9			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f =1 kHz, Av = 1, R_L= 10 kΩ, BW = 22 kHz, V_{in}= 0.8 V_{PP}		0.001		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

Table 4. Electrical characteristics at V_{CC+} = 10 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io} (TSX711, TSX712)	Input offset voltage	V_{icm} = V_{CC}/2			200	µV
		T_{min} < T_{op} < 85 °C			365	
		T_{min} < T_{op} < 125 °C			450	
V_{io} (TSX711A)		V_{icm} = V_{CC}/2			100	
		T_{min} < T_{op} < 85 °C			265	
		T_{min} < T_{op} < 125 °C			350	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		25		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current(1)	V_{out} = V_{CC}/2		1	50	pA
		T_{min} < T_{op} < T_{max}			200	
I_{io}	Input offset current(1)	V_{out} = V_{CC}/2		1	50	
		T_{min} < T_{op} < T_{max}			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR (TSX711, TSX711A)	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 10.1 V, V_{out} = V_{CC}/2	90	102		dB
		T_{min} < T_{op} < T_{max}	86			
		V_{icm} = -0.1 to 8 V, V_{out} = V_{CC}/2	105	117		
		T_{min} < T_{op} < T_{max}	95			
CMRR (TSX712)		V_{icm} = -0.1 to 10.1 V, V_{out} = V_{CC}/2	88	100		
		T_{min} < T_{op} < T_{max}	84			
		V_{icm} = -0.1 to 8 V, V_{out} = V_{CC}/2	98	106		
		T_{min} < T_{op} < T_{max}	92			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out} = 0.3 to 9.7 V	110	140		
		T_{min} < T_{op} < T_{max}	100			
		R_L = 10 kΩ, V_{out} = 0.2 to 9.8 V	110			
		T_{min} < T_{op} < T_{max}	100			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L = 2 kΩ o V_{CC}/2		45	70	mV
		T_{min} < T_{op} < T_{max}			80	
		R_L = 10 kΩ o V_{CC}/2		10	30	
		T_{min} < T_{op} < T_{max}			40	
V_{OL}	Low level output voltage	R_L = 2 kΩ o V_{CC}/2		42	70	
		T_{min} < T_{op} < T_{max}			80	
		R_L = 10 kΩ o V_{CC}/2		9	30	
		T_{min} < T_{op} < T_{max}			40	
I_{out} (TSX711, TSX711A)	I_{sink}	V_{out} = V_{CC}	50	70		mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out} (TSX711, TSX711A)	I_{sink}	$T_{min} < T_{op} < T_{max}$	40			mA
	I_{source}	V_{out} = 0 V	50	69		
		$T_{min} < T_{op} < T_{max}$	40			
I_{out} (TSX712)	I_{sink}	$V_{out} = V_{CC}$	30	39		
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	50	69		
		$T_{min} < T_{op} < T_{max}$	40			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}/2$		630	850	µA
		$T_{min} < T_{op} < T_{max}$			1000	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		53		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 8 V_{PP}, 10 % to 90 %	0.8	1		V/µs
		$T_{min} < T_{op} < T_{max}$	0.7			
SRp	Positive slew rate	Av = 1, V_{out} = 8 V_{PP}, 10 % to 90 %	1.0	1.3		
		$T_{min} < T_{op} < T_{max}$	0.9			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, BW = 22 kHz, V_{in} = 5 V_{PP}		0.0003		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

Table 5. Electrical characteristics at V_{CC+} = 16 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L > 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io} (TSX711, TSX712)	Input offset voltage	$V_{icm} = V_{CC}/2$			200	µV
		$T_{min} < T_{op} < 85$ °C			365	
		$T_{min} < T_{op} < 125$ °C			450	
V_{io} (TSX711A)		$V_{icm} = V_{CC}/2$			100	
		$T_{min} < T_{op} < 85$ °C			265	
		$T_{min} < T_{op} < 125$ °C			350	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)				2.5	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		500		$\frac{nV}{\sqrt{month}}$
I_{ib}	Input bias current(1)	$V_{out} = V_{CC}/2$		1	50	pA
		$T_{min} < T_{op} < T_{max}$			200	
I_{io}	Input offset current(1)	$V_{out} = V_{CC}/2$		1	50	
		$T_{min} < T_{op} < T_{max}$			200	
R_{IN}	Input resistance			1		TΩ
C_{IN}	Input capacitance			12.5		pF
CMRR (TSX711, TSX711A)	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	V_{icm} = -0.1 to 16.1 V, $V_{out} = V_{CC}/2$	94	113		dB
		$T_{min} < T_{op} < T_{max}$	90			
		V_{icm} = -0.1 to 14 V, $V_{out} = V_{CC}/2$	110	116		
		$T_{min} < T_{op} < T_{max}$	96			
CMRR (TSX712)		V_{icm} = -0.1 to 16.1 V, $V_{out} = V_{CC}/2$	94	107		
		$T_{min} < T_{op} < T_{max}$	90			
		V_{icm} = -0.1 to 14 V, $V_{out} = V_{CC}/2$	100	107		
		$T_{min} < T_{op} < T_{max}$	90			
SVRR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 4 to 16 V	100	131		
		$T_{min} < T_{op} < T_{max}$	90			
A_{vd}	Large signal voltage gain	R_L = 2 kΩ, V_{out} = 0.3 to 15.7 V	110	146		
		$T_{min} < T_{op} < T_{max}$	100			
		R_L = 10 kΩ, V_{out} = 0.2 to 15.8 V	110	149		
		$T_{min} < T_{op} < T_{max}$	100			
V_{OH}	High level output voltage (voltage drop from V_{CC+})	R_L = 2 kΩ (TSX711, TSX711A)		100	130	mV
		R_L = 2 kΩ (TSX712)		70	130	
		$T_{min} < T_{op} < T_{max}$			150	
		R_L = 10 kΩ		16	40	
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low level output voltage	R_L = 2 kΩ		70	130	mV
		$T_{min} < T_{op} < T_{max}$			150	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	R_L = 10 kΩ		15	40	mV
		$T_{min} < T_{op} < T_{max}$			50	
I_{out} (TSX711, TSX711A)	I_{sink}	$V_{out} = V_{CC}$	50	71		mA
		$T_{min} < T_{op} < T_{max}$	45			
	I_{source}	V_{out} = 0 V	50	68		
		$T_{min} < T_{op} < T_{max}$	45			
I_{out} (TSX712)	I_{sink}	$V_{out} = V_{CC}$	30	40		
		$T_{min} < T_{op} < T_{max}$	15			
	I_{source}	V_{out} = 0 V	50	68		
		$T_{min} < T_{op} < T_{max}$	45			
I_{CC}	Supply current per amplifier	No load, $V_{out} = V_{CC}/2$		660	900	µA
		$T_{min} < T_{op} < T_{max}$			1000	
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.9	2.7		MHz
ϕm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L= 100 pF		15		dB
SRn	Negative slew rate	Av = 1, V_{out} = 10 V_{PP}, 10 % to 90 %	0.7	0.95		V/µs
		$T_{min} < T_{op} < T_{max}$	0.6			
SRp	Positive slew rate	Av = 1, V_{out} = 10 V_{PP}, 10 % to 90 %	1	1.4		
		$T_{min} < T_{op} < T_{max}$	0.9			
e_n	Equivalent input noise voltage	f = 1 kHz		22		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		19		
THD+N	Total harmonic distortion + Noise	f = 1 kHz, Av = 1, R_L = 10 kΩ, BW = 22 kHz, V_{in} = 5 V_{PP}		0.0002		%

1. *Maximum values are guaranteed by design.*
2. *Typical value is based on the Vio drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration (see Section 5.6 Long term input offset voltage drift).*

4 Electrical characteristic curves

Figure 2. Supply current vs. supply voltage

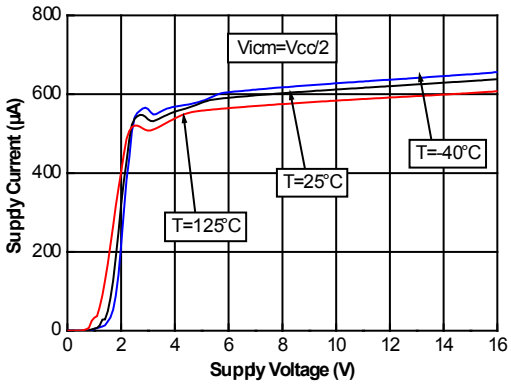


Figure 3. Input offset voltage distribution at V_{CC} = 16 V

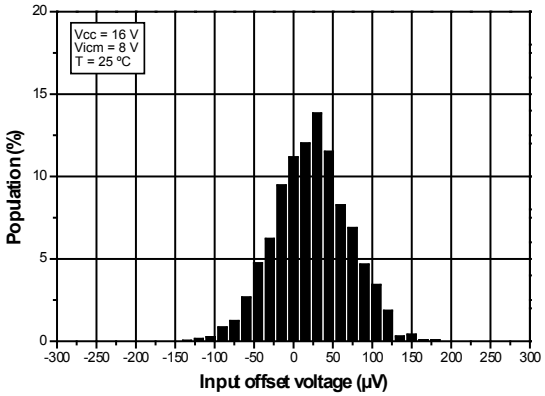


Figure 4. Input offset voltage distribution at V_{CC} = 4 V

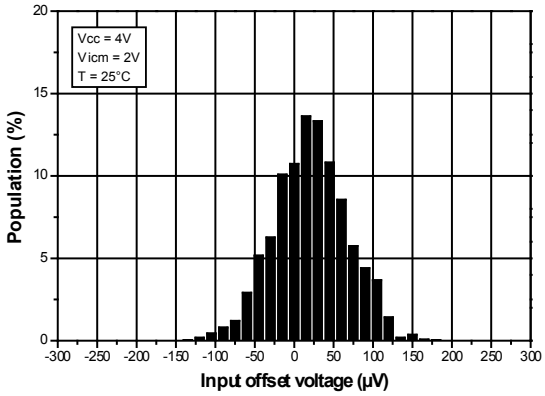


Figure 5. Input offset voltage vs. temperature at V_{CC} = 16 V

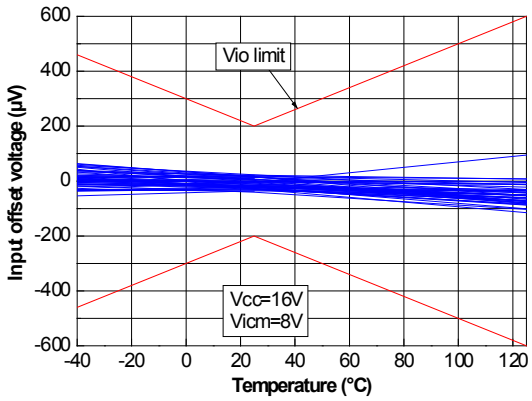


Figure 6. Input offset voltage drift population

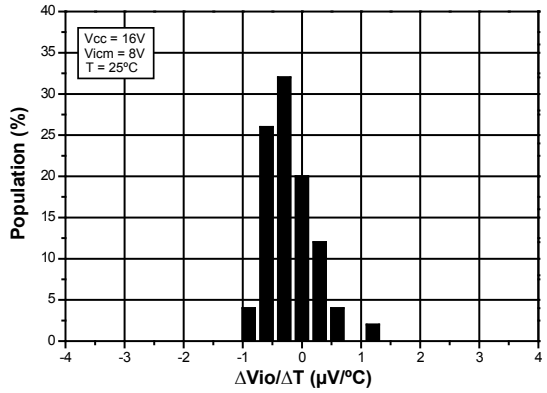


Figure 7. Input offset voltage vs. supply voltage at V_{ICM} = 0 V

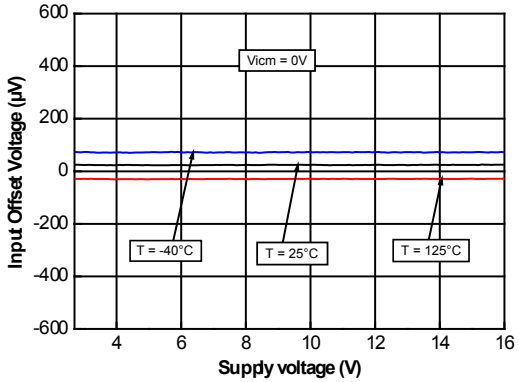


Figure 8. Input offset voltage vs. common mode voltage at V_{CC} = 2.7 V

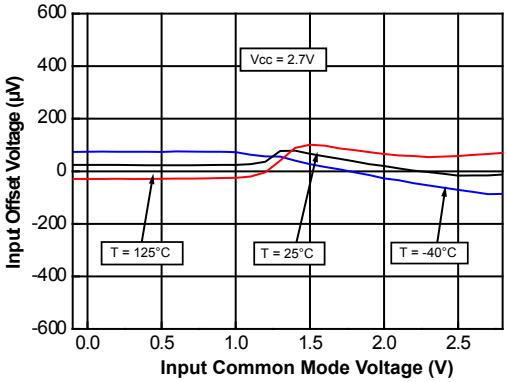


Figure 9. Input offset voltage vs. common mode voltage at V_{CC} = 16 V

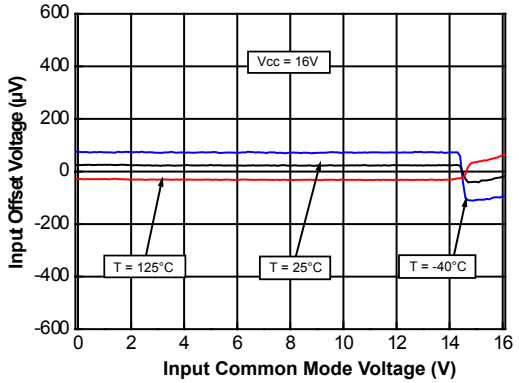


Figure 10. Output current vs. output voltage at V_{CC} = 2.7 V (TSX711, TSX711A)

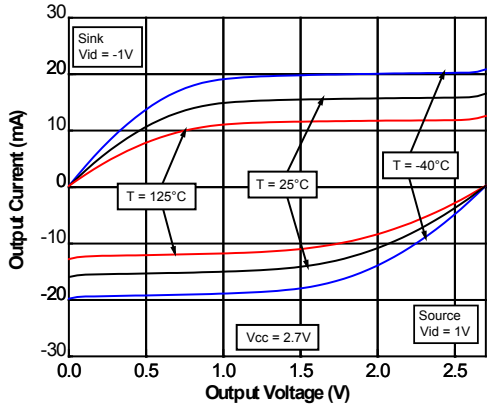


Figure 11. Output current vs. output voltage at V_{CC} = 16 V (TSX711, TSX711A)

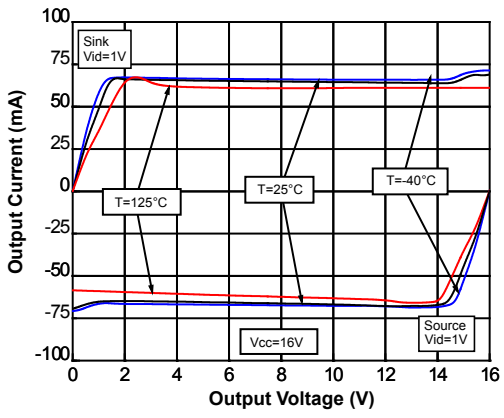


Figure 12. Output current vs. output voltage at V_{CC} = 2.7 V (TSX712)

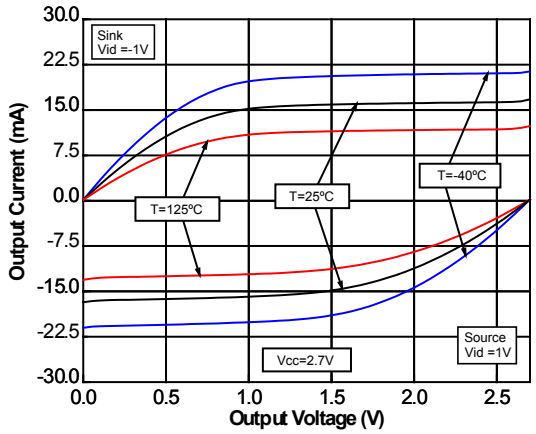


Figure 13. Output current vs. output voltage at V_{CC} = 16 V (TSX712)

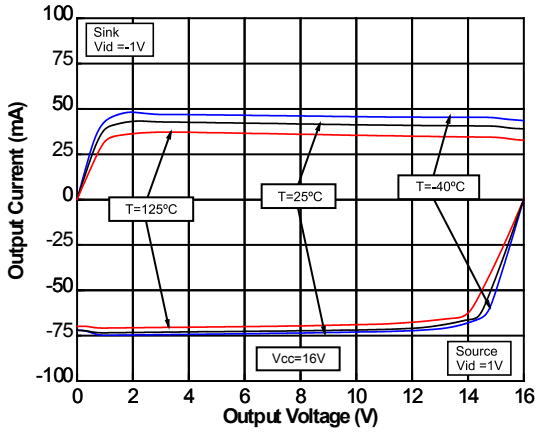


Figure 14. Output low voltage vs. supply voltage

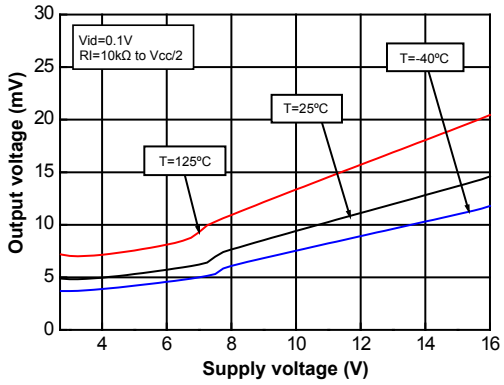


Figure 15. Output high voltage (drop from V_{CC+}) vs. supply voltage

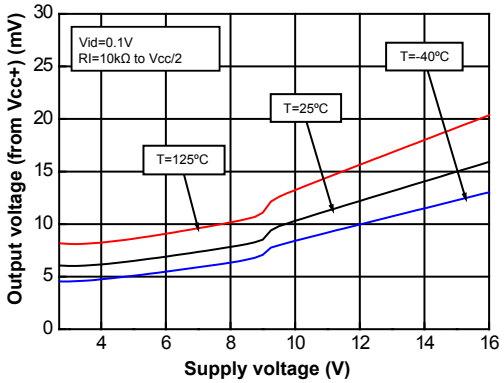


Figure 16. Output voltage vs. input voltage close to the rail at V_{CC} = 16 V

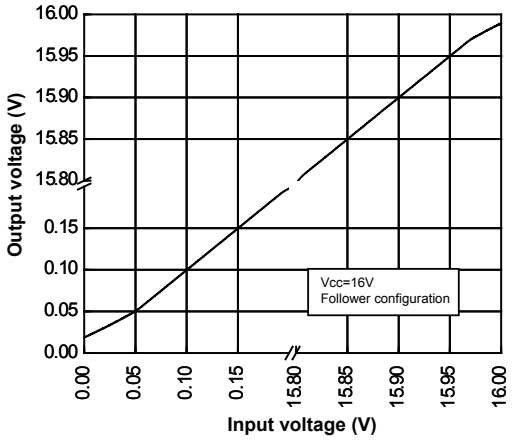


Figure 17. Slew rate vs. supply voltage

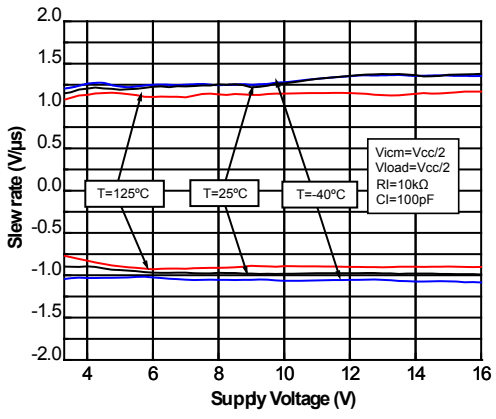


Figure 18. Negative slew rate at V_{CC} = 16 V

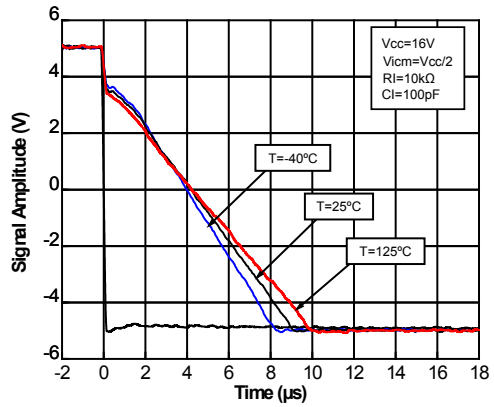


Figure 19. Positive slew rate at V_{CC} = 16 V

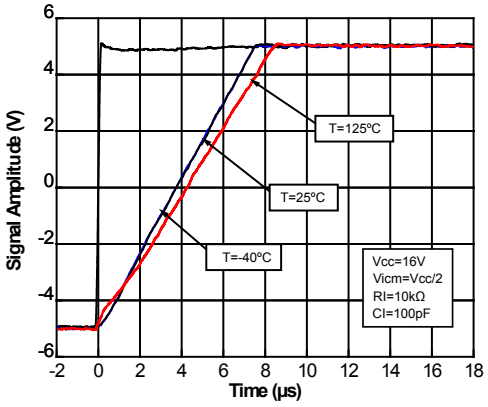


Figure 20. Response to a small input voltage step

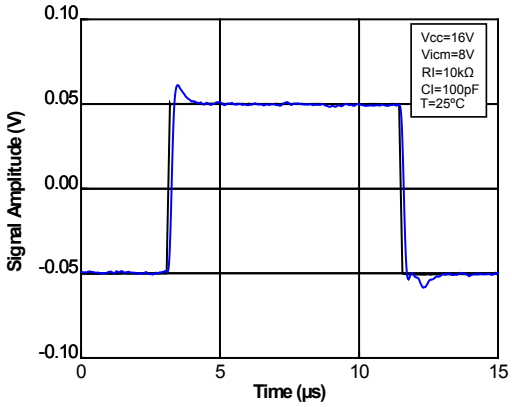


Figure 21. Recovery behavior after a negative step on the input

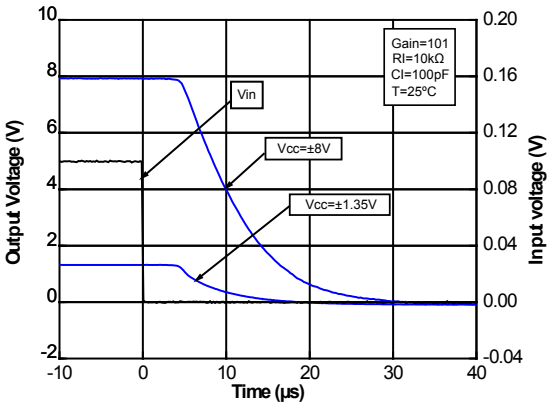


Figure 22. Recovery behavior after a positive step on the input

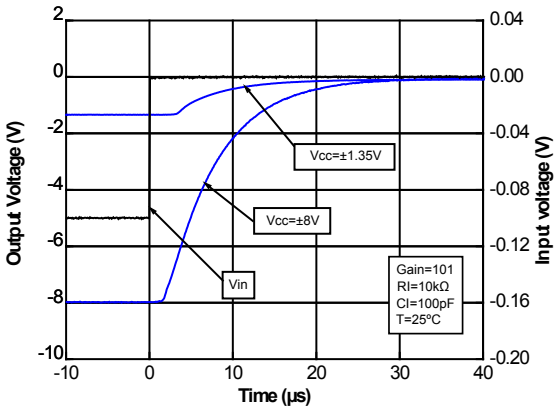


Figure 23. Bode diagram at V_{CC} = 2.7 V

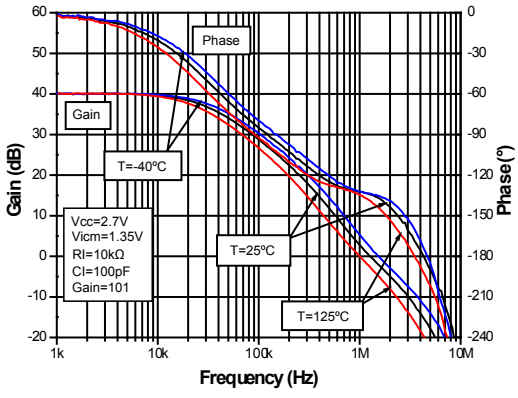


Figure 24. Bode diagram at V_{CC} = 16 V

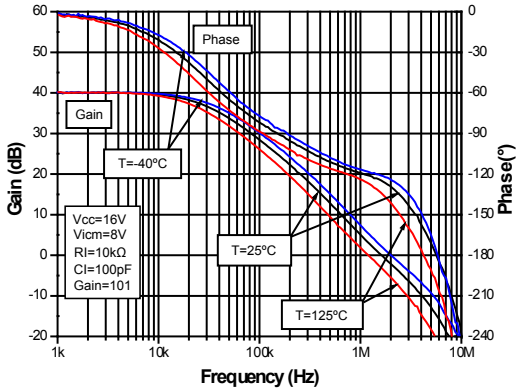


Figure 25. Power supply rejection ratio (PSRR) vs. frequency

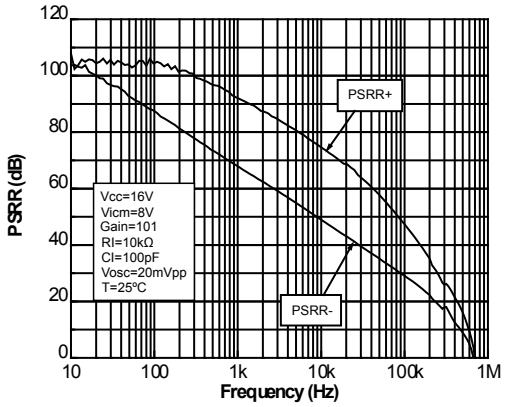


Figure 26. Output overshoot vs. capacitive load

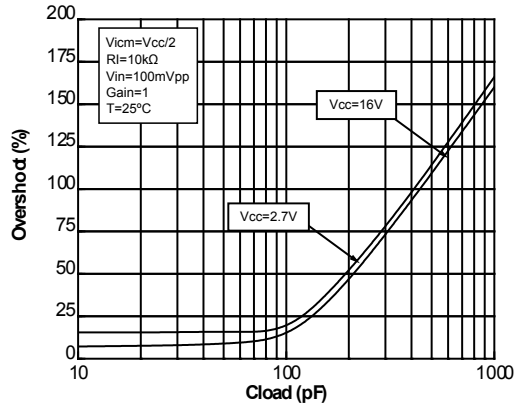


Figure 27. Output impedance vs. frequency in closed loop configuration

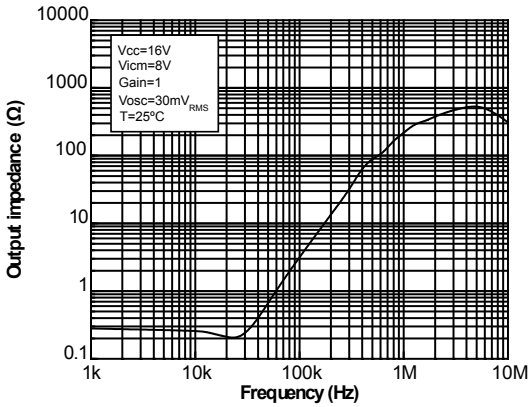


Figure 28. THD + N vs. frequency

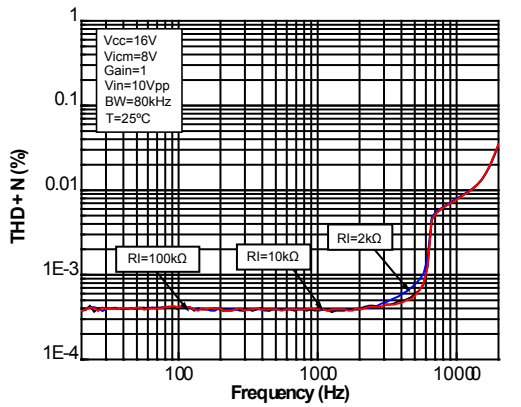


Figure 29. THD + N vs. output voltage

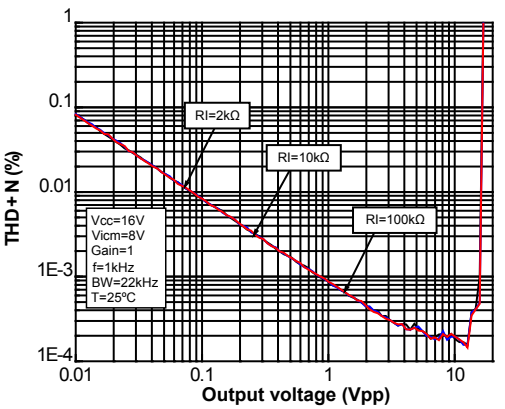


Figure 30. **Noise vs. frequency**

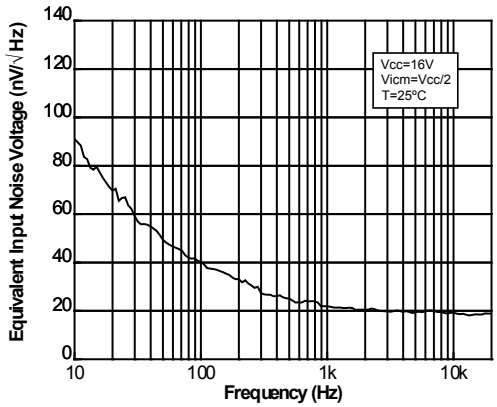


Figure 31. **0.1 to 10Hz noise**

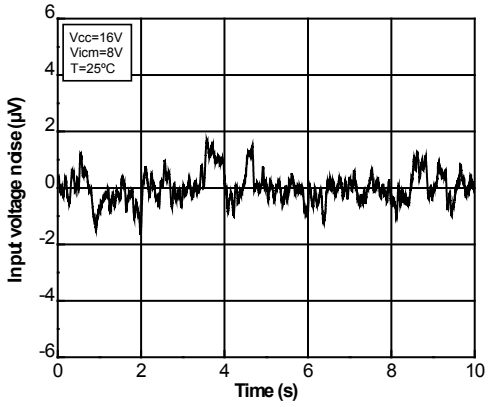
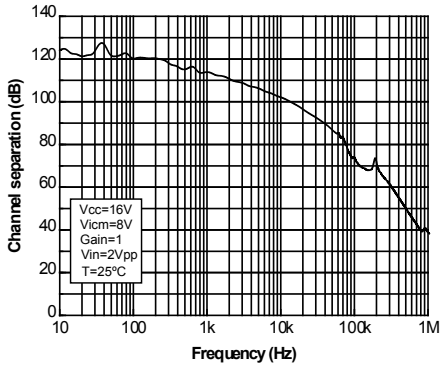


Figure 32. **Channel separation (TSX712)**



5 Application information

5.1 Operating voltages

The TSX711, TSX711A, and TSX712 devices can operate from 2.7 to 16 V. The parameters are fully specified for 4 V, 10 V, and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

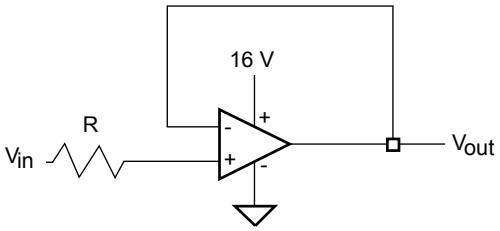
5.2 Input pin voltage ranges

The TSX711, TSX711A, and TSX712 devices have internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this overcurrent can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as described in Figure 33. Input current limitation.

Figure 33. Input current limitation



5.3 Rail-to-rail input

The TSX711, TSX711A, and TSX712 devices have a rail-to-rail input, and the input common mode range is extended from ($V_{CC\ -}$) - 0.1 V to (V_{CC+}) + 0.1 V.

5.4 Rail-to-rail output

The operational amplifier output levels can go close to the rails: to a maximum of 40 mV above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

5.5 Input offset voltage drift overtemperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using Equation 1.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 125 °C.

The TSX711, TSX711A, and TSX712 datasheet maximum values are guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.6 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Equation 2.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die undertemperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\ \text{h} \times 12\ \text{months} / (24\ \text{h} \times 365.25\ \text{days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 6).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7).

Equation 7

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{(months)}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.7 High values of input differential voltage

In a closed loop configuration, which represents the typical use of an op amp, the input differential voltage is low (close to V_{io}). However, some specific conditions can lead to higher input differential values, such as:

- operation in an output saturation state
- operation at speeds higher than the device bandwidth, with output voltage dynamics limited by slew rate
- use of the amplifier in a comparator configuration, hence in open loop.

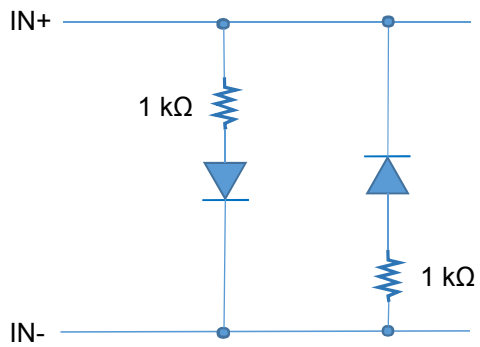
Use of the TSX711, TSX711A, or TSX712 in comparator configuration, especially combined with high temperature and long duration can create a permanent drift of V_{io}.

5.7.1 Input stage protection

In order to protect the input stage against large differential voltage, the TSX71x, have internal back to back protection diodes between both inputs.

In order to limit the current flowing through these diodes, 1 kΩ serial resistances are placed in series with these diodes, as described in Figure 34.

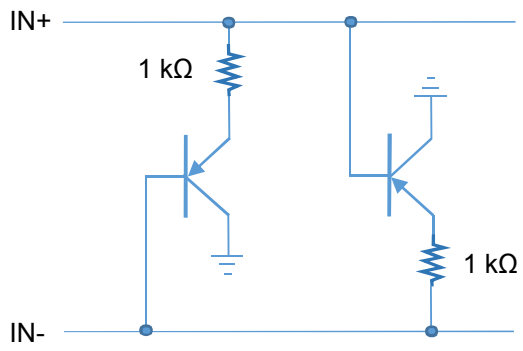
Figure 34. Differential input protection



A maximum differential voltage of 18 V is allowed, as mentioned by Table 1, so a bit less than 18 mA maximum current can flow through the diodes, which represent a safe condition for such diodes.

The protection diodes are made with PNP transistor as described by Figure 35.

Figure 35. Differential input protection (PNP)

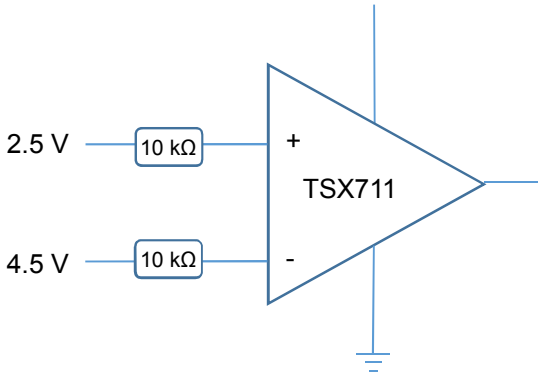


As a result, the amount of current flowing into the diodes, when a large differential input voltage is applied, is not symmetrical (different current on IN+ and IN- pins).

Indeed, when the differential input voltage becomes high enough to have one transistor in active region (forward biased base-emitter junction), the second one is off (as its base-emitter junction is reversed biased). The current is flowing from the input pin with the highest voltage directly to GND (Vcc-) through the resistor and the transistor. Only a small part of it is flowing to the input pin with the lowest voltage thanks to the gain (beta) of the transistor.

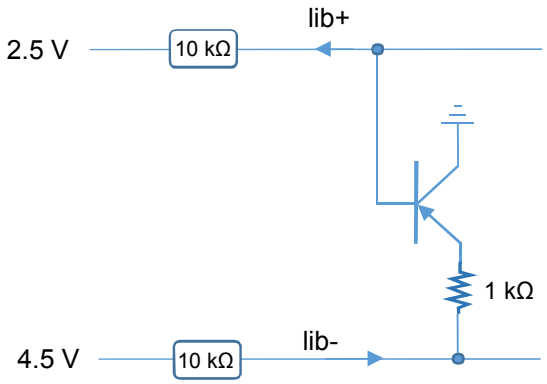
The following example explains how the current can flow. Let's consider the TSX711 used as a comparator mode as described by Figure 36. TSX711 in comparator mode (the 10 kΩ resistors are added at application level).

Figure 36. TSX711 in comparator mode



The TSX711 input can be described by Figure 37. TSX711 input in comparator mode.

Figure 37. TSX711 input in comparator mode



As the differential voltage on input pins becomes higher than the forward voltage of the emitter-base junction (~ 0.7 V), the PNP transistor is forward active. The current drawn on input pin IN- is:

$$Iib- = \frac{4.5V - 2.5V - Vbe}{10k\Omega + 1k\Omega + 10k\Omega/(\beta+1)} \approx \frac{2V - Vbe}{11k\Omega} \approx 120\mu A$$

and $Iib+ = \frac{Iib-}{\beta+1}$, is in the range of the µA.

So, when it is used in the nonlinear region, the current on the input pins can be different from the pin IN+ and pin IN-. And this current is directly linked to the differential voltage applied on the input pins and the serial resistance added in the input path.

5.8 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, the unity gain configuration is the worst case for stability and the ability to drive large capacitive loads.

Figure 38. Stability criteria with a serial resistor at different supply voltage shows the serial resistor that must be added to the output, to make a system stable. Figure 39. Test configuration for Riso shows the test configuration using an isolation resistor, Riso.

Figure 38. Stability criteria with a serial resistor at different supply voltage

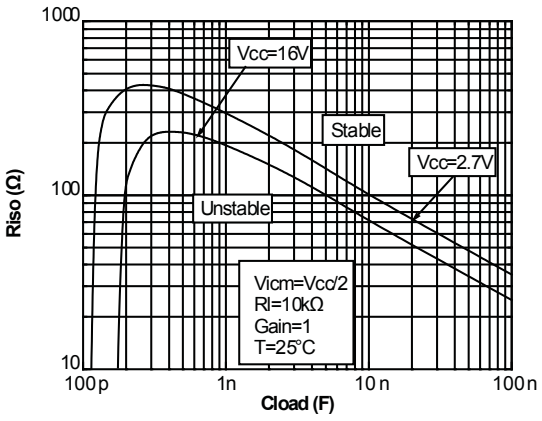
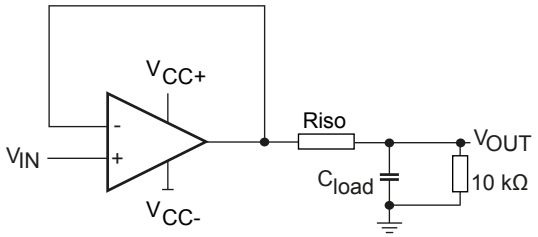


Figure 39. **Test configuration for Riso**



5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB, tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Optimized application recommendation

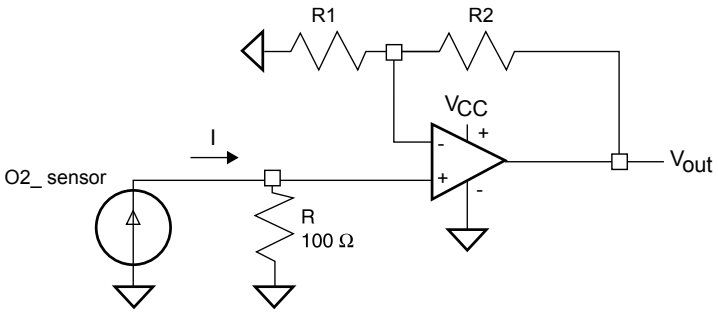
It is recommended to place a 22 nF capacitor as close as possible to the supply pin. A good decoupling helps to reduce electromagnetic interference impact.

5.11 Application examples

5.11.1 Oxygen sensor

The electrochemical sensor creates a current proportional to the concentration of the gas being measured. This current is converted into voltage thanks to R resistance. This voltage is then amplified by the TSX711, TSX711A, or the TSX712 (see Figure 40. Oxygen sensor principle schematic).

Figure 40. **Oxygen sensor principle schematic**



The output voltage is calculated using Equation 8:

Equation 8

$$V_{out} = (I \times R - V_{io}) \times \left(\frac{R_2}{R_1} + 1\right)$$

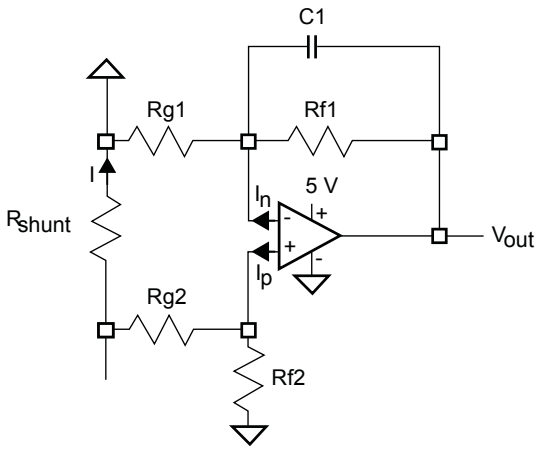
As the current delivered by the O2 sensor is extremely low, the impact of the V_{io} can become significant with a traditional operational amplifier. The use of a precision amplifier like the TSX711, TSX711A, TSX712 is perfect for this application.

In addition, using the TSX711, TSX711A, TSX712 for the O2 sensor application ensures that the measurement of O2 concentration is stable, even at different temperatures, thanks to a small $\Delta V_{io}/\Delta T$.

5.11.2 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSX711, TSX711A, or TSX712 (see Figure 41. Low-side current sensing schematic).

Figure 41. Low-side current sensing schematic



V_{out} can be expressed as follows:

Equation 9

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2} \times R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \times R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Equation 9 can be simplified as follows:

Equation 10

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

The main advantage of using a precision amplifier like the TSX711, TSX711A, or TSX712, for a low-side current sensing, is that the errors due to V_{io} and I_{io} are extremely low and may be neglected.

Therefore, for the same accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost.

Particular attention must be paid on the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

Taking into consideration the resistor inaccuracies, the maximum and minimum output voltage of the operational amplifier can be calculated respectively using Equation 11 and Equation 12.

Equation 11

$$\text{Maximum Vout} = \text{Rshunt} \times \text{I} \times \left(\frac{\text{Rf}}{\text{Rg}}\right) \times (1 + \varepsilon\text{rs} + 2\varepsilon\text{r}) + \text{Vio} \times \left(1 + \frac{\text{Rf}}{\text{Rg}}\right) + \text{Rf} \times \text{Iio}$$

Equation 12

$$\text{Minimum Vout} = \text{Rshunt} \times \text{I} \times \left(\frac{\text{Rf}}{\text{Rg}}\right) \times (1 - \varepsilon\text{rs} - 2\varepsilon\text{r}) - \text{Vio} \times \left(1 + \frac{\text{Rf}}{\text{Rg}}\right) + \text{Rf} \times \text{Iio}$$

Where:

- εrs is the shunt resistor inaccuracy (example, 1 %)
- εr is the inaccuracy of the Rf and Rg resistors (example, 0.1 %)

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 42. SOT23-5 package outline

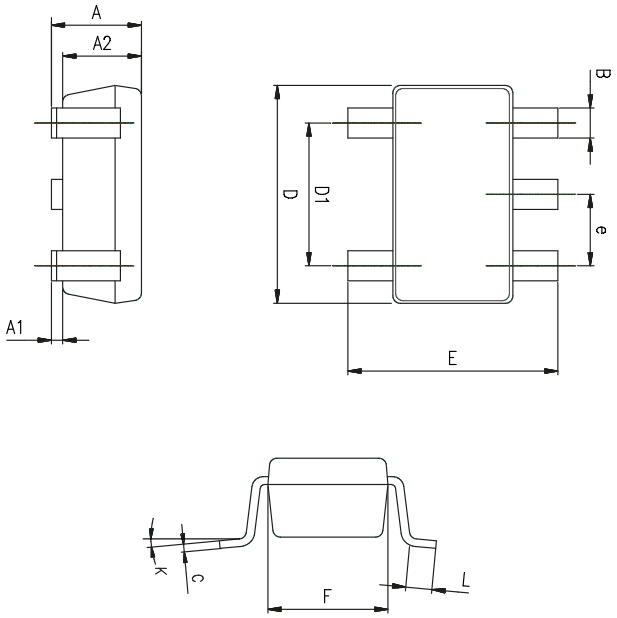


Table 6. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 MiniSO8 package information

Figure 43. **MiniSO8 package outline**

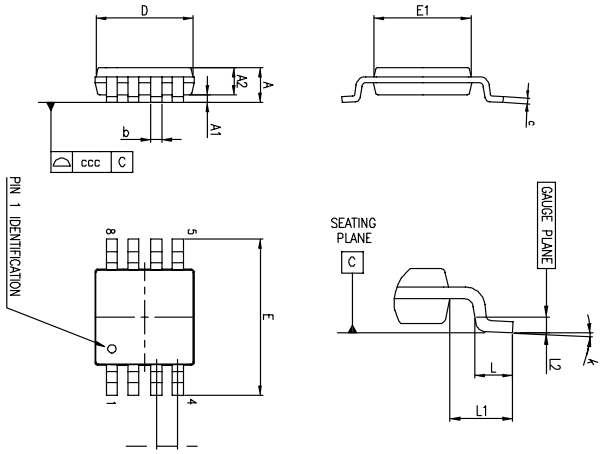


Table 7. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.3 SO8 package information

Figure 44. **SO8 package outline**

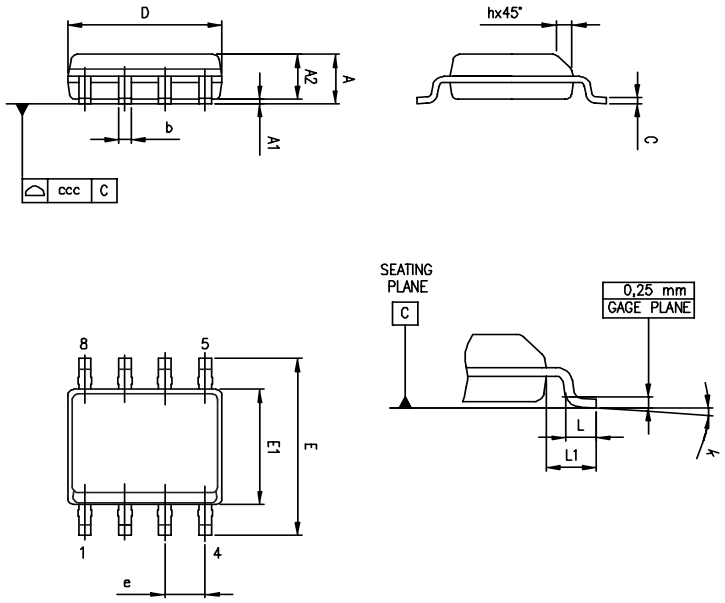


Table 8. **SO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

7 Ordering information

Table 9. Order codes

Order code	Temperature range	Package	Packaging	Marking
TSX711ILT	-40 to 125 °C	SOT23-5	Tape and reel	K29
TSX711AILT				K195
TSX711IYLT (1)	-40 to 125 °C (automotive grade)			K197
TSX711AIYLT (1)				K198
TSX712IDT	-40 to 125 °C	SO8		TSX712
TSX712IST		MiniSO8		K211
TSX712IYDT (1)	-40 to 125 °C (automotive grade)	SO8		TSX712Y
TSX712IYST (1)		MiniSO8		K212

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
27-Feb-2014	1	Initial release
19-Mar-2014	2	Table 1: updated ESD data for MM (machine model)
25-Jul-2014	3	Table 3: updated I_{out} (I_{sink}) values. Table 3, Table 4, and Table 5: updated V_{io} values, updated $\Delta V_{io}/\Delta T$. Table 5: updated V_{OL} values Table 6: updated “inches” dimensions
26-Jan-2016	4	TSX711 datasheet merged with TSX712 datasheet. Reworked the following sections: Cover image, Related products, Description, Section 1: "Package pin connections", Section 2: "Absolute maximum ratings and operating conditions", Section 3: "Electrical characteristics", Section 4: "Electrical characteristic curves", Section 5.1: "Operating voltages", Section 5.2: "Input pin voltage ranges", Section 5.3: "Rail-to-rail input", Section 5.4: "Rail-to-rail output", Section 5.5: "Input offset voltage drift over temperature", Section 5.7: "High values of input differential voltage", Section 5.11.1: "Oxygen sensor", Section 5.11.2: "Low-side current sensing", Section 7: "Ordering information". Added: Section 6.2: "MiniSO8 package information" and Section 6.3: "SO8 package information".
21-Mar-2017	5	Added part number TSX711A Table 9: "Order codes": updated footnotes with respect to TSX711IYLT, TSX711AIYLT, TSX712IYDT, and TSX712IYST.
22-Sep-2020	6	Added new Section 5.7.1 Input stage protection.