T-46-07-11

National Semiconductor

74FCT373A
Octal Transparent Latch with TRI-STATE® Outputs

General Description

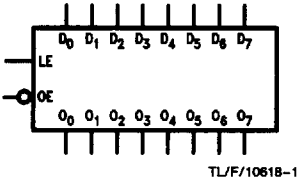
The 'FCT373A consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

- I_{CC} and I_{OZ} reduced to 40.0 μA and ±2.5 μA respectively
- NSC 74FCT373A pin and functionally equivalent to IDT 74FCT373A
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- TTL input and output level compatible
- High current latch up immunity
- I_{OL} = 48 mA

Ordering Code: See Section 8

Logic Symbols



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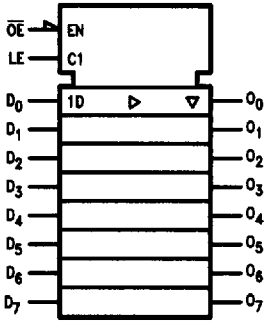

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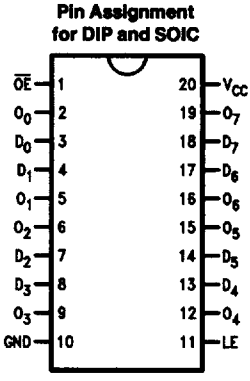
Connection Diagram



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Functional Description

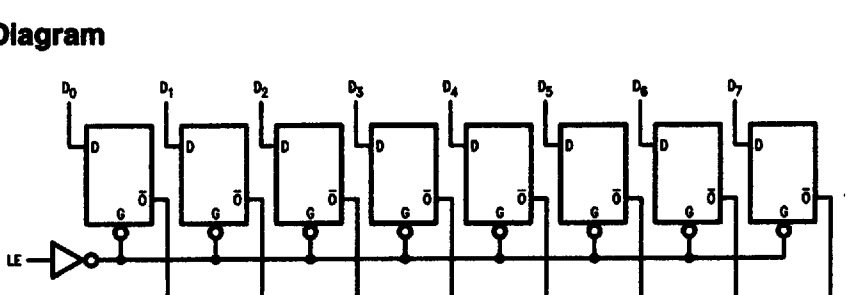
The 'FCT373A contains eight D-type latches with TRI-STATE outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
74FCTA −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
74FCTA −55°C to +125°C

Storage Temperature (T_{STG})
74FCTA −55°C to +125°C

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCTA circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCTA 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
74FCTA −0°C to +70°C

Junction Temperature (T_J)
PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	74FCTA Min	74FCTA Typ	74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			2.5 2.5 −2.5 −2.5	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4	V_{CC} 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −15 mA
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3	0.2 0.50		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA
I_{CC}	Maximum Quiescent Supply Current		1.0	40.0	μA	V_{CC} = Max V_{IN} ≥ V_{HC}, V_{IN} ≤ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74FCTA $T_A = +25°C$ $V_{CC} = 5.0V$	74FCTA $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	4.0	1.5	5.2	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5	ns	2-11
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	7.0	2.0	8.5	ns	2-8
t_{SU}	Set Up Time High or Low D_n to LE	1.0	2.0		ns	2-10
t_H	Hold Time High or Low D_n to LE	1.0	1.5		ns	2-10
t_w	LE Pulse Width High or Low	4.0	5.0		ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C$, f = 1.0 MHz

Symbol	Parameter (Note 1)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.