CDx4AC245, CDx4ACT245 Octal-Bus Transceiver, Three-State, Non-Inverting

1 Features

- Buffered inputs
- Typical propagation delay
  - 4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ± 24 mA output drive current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω transmission line

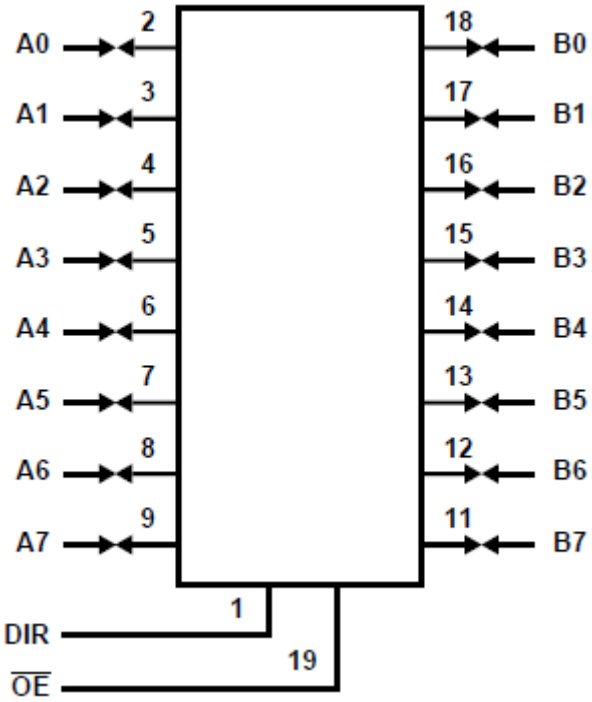
2 Description

The 'AC245 and 'ACT245 are octal-bus transceivers that utilize Advanced CMOS Logic technology.

Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
CD74AC245/ CD74ACT245	N (PDIP, 20)	24.33 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
CD54AC245/ CD54ACT245	J (CDIP, 20)	24.2 mm × 6.92 mm
CD74ACT245	DB (SSOP, 20)	7.2 mm × 5.3 mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2002) to Revision C (May 2023)	Page
• Added *Package Information* table, *Pin Functions* table, and *Thermal Information* table	1

4 Pin Configuration and Functions

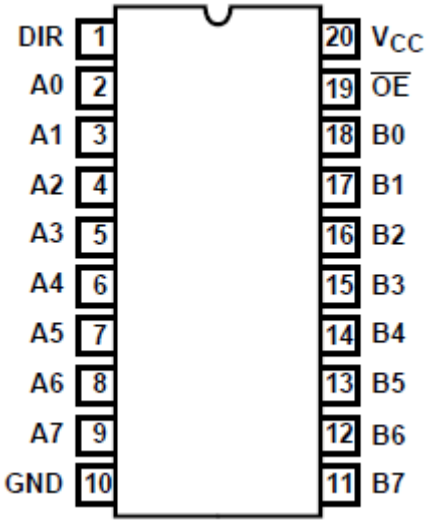


Figure 4-1. CD54AC245, CD54ACT245 (CERDIP), CD74AC245, CD74ACT245 (PDIP, SOIC, SSOP) Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction Pin
2	A0	I/O	A1 Input/Output
3	A1	I/O	A2 Input/Output
4	A2	I/O	A3 Input/Output
5	A3	I/O	A4 Input/Output
6	A4	I/O	A5 Input/Output
7	A5	I/O	A6 Input/Output
8	A6	I/O	A7 Input/Output
9	A7	I/O	A8 Input/Output
10	GND	—	Ground Pin
11	B7	I/O	B7 Input/Output
12	B6	I/O	B6 Input/Output
13	B5	I/O	B5 Input/Output
14	B4	I/O	B4 Input/Output
15	B3	I/O	B3 Input/Output
16	B2	I/O	B2 Input/Output
17	B1	I/O	B1 Input/Output
18	B0	I/O	B0 Input/Output
19	$\overline{OE}$	I/O	Output Enable
20	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6	V
I_{IK}	Input diode current	V_I < -0.5V or V_I > V_{CC} + 0.5V		± 20	mA
I_{OK}	Output diode current	V_O < -0.5V or V_O > V_{CC} + 0.5V		± 50	mA
I_O	Output source or sink current per output pin	V_O > -0.5V or V_O < V_{CC} + 0.5V		± 50	mA
I_{OK}	V_{CC} or ground current	I_{CC} or I_{GND}		± 100	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			CDx4AC245		CDx4ACT245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage[3]		1.5V	5.5V	4.5V	5.5V	V
V_I, V_O	Input or Output Voltage		0V	V_{CC}	0V	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate	1.5V to 3V		50			ns
		3.6V to 5.5V		20			
		4.5V to 5.5V				10	
T_A	Temperature range		–55	125	–55	125	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.3 Thermal Information

THERMAL METRIC(1)		CDx4AC14/ CDx4ACT14			UNIT
		E	M	SM	
		20 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69	58	70	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
V_{IH}	High-level input voltage			1.5	1.2		1.2		1.2		V
				3	2.1		2.1		2.1		
				5.5	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{IL}		1.5		0.3		0.3		0.3	V
				3		0.9		0.9		0.9	
				5.5		1.65		1.65		1.65	
V_{OH}	High-level output voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4		1.4		1.4		VV_{OH}
			-0.05	3	2.9		2.9		2.9		
			-0.05	4.5	4.4		4.4		4.4		
			-4	3	2.58		2.48		2.4		
			-24	4.5	3.94		3.8		3.7		
			-75	5.5			3.85				
			-50	5.5					3.85		
V_{OL}	Low-level output voltage	V_{IH} or V_{IL}	0.05	1.5 V		0.1		0.1		0.1	V
			0.05	3 V		0.1		0.1		0.1	
			0.05	4.5 V		0.1		0.1		0.1	
			12	3 V		0.36		0.44		0.5	
			24	4.5 V		0.36		0.44		0.5	
			75[1]	5.5 V				1.65			
			50[1]	5.5 V						1.65	
I_I	Input leakage current	V_{CC} or GND		5.5		± 0.1		± 1		± 1	μ A
I_{OZ}	Three-state leakage current	V_{IH} or V_{IL}, VO = V_{CC} or GND		5.5 V		± 0.5		± 5		± 10	μ A
I_{CC}	Quiescent supply current MSI	V_{CC} or GND	0	5.5 V		8		80		160	μ A
ACT TYPES											
V_{IH}	High-level input voltage			4.5 V to 5.5 V	2		2		2		V
V_{IL}	Low-level input voltage			4.5 V to 5.5 V		0.8		0.8		0.8	V
V_{OH}	High-level output voltage	V_{IH} or V_{IL}	-0.05	4.5 V	4.4		4.4		4.4	0.8	V
			-24	4.5 V	3.94		3.8		3.7		
			-75[1]	5.5 V			3.85				
			-50	5.5 V					3.85		

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Low-level output voltage	V_{IH} or V_{IL}	0.05	4.5		0.1		0.1		0.1	V
			24	4.5		0.36		0.44		0.5	
			75[1]	5.5				1.65			
			50[1]	5.5						1.65	
											V
I_I	Input leakage current	V_{CC} or GND		5.5 V		± 0.1		± 1		± 1	µA
I_{OZ}	Three-state or leakage current	V_{IH} or $V_{IL}V_O$ = V_{CC} or GND		5.5 V		± 0.5		± 5		± 10	µA
I_{CC}	Quiescent supply current MSI	V_{CC} or GND	0	5.5 V		8		80		160	µA
Δ I_{CC}	Additional supply current per input pin TTL inputs high 1 unit load	V_{CC} -2.1		4.5 to 5.5		2.4		2.8		3	mA

1. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

5.5 Switching Characteristics

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
t_{PLH}, t_{PHL}	Propagation delay, data to output	1.5			96			106	ns
		3.3		3.2	10.8	3		11.9	
		5		2.2	7.7	2.1		8.5	
t_{PLZ}, t_{PHZ}	Propagation delay, output disable to output	1.5			159			175	ns
		3.3		4.7	15.9	4.4		17.5	
		5		3.7	12.7	3.5		14	
t_{PZL}, t_{PZH}	Propagation delay, output enable to output	1.5			159			175	ns
		3.3		5.6	19	5.3		21	
		5		3.7	12.7	3.5			
V_{OHV}	Minimum (Valley) V_{OH} During switching of other outputs (output under test not switching)	5		4 at 25°C			4 at 25°C		V

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OLP}	Maximum (Peak) V_{OL} During switching of other outputs (output under test not switching)	5		1 at 25°C			1 at 25°C		V
C_O	Three-state output capacitance			15			15		pF
C_I	Input capacitance				10			10	pF
C_{PD}	Power dissipation capacitance			57			57		pF
ACT TYPES									
t_{PLH}, t_{PHL}	Propagation delay, data to output	5	2.7		9.1	2.5		10	ns
t_{PLZ}, t_{PHZ}	Propagation delay, output disable to output	5	3.7		12.7	3.5		14	ns
t_{PZL}, t_{PZH}	Propagation delay, output enable to output	5	3.8		13.1	3.6		14.4	ns
V_{OHV}	Minimum (Valley) V_{OH} During switching of other outputs (output under test not switching)	5		4 at 25°C			4 at 25°C		V
V_{OLP}	Maximum (Peak) V_{OL} During switching of other outputs (output under test not switching)	5		1 at 25°C			1 at 25°C		V
C_O	Three-state output capacitance			15			15		pF
C_I	Input capacitance				10			10	pF
C_{PD}	Power dissipation capacitance			57			57		pF

1. Limits tested 100%
2. 3.3V Min is at 3.6V, Max is at 3V
3. 5V Min is at 5.5V, Max is at 4.5V
4. CPD is used to determine the dynamic power consumption per channel
   - AC: PD = VCC2 fi (CPD + CL)
   - ACT: PD = VCC2 fi (CPD + CL) + VCC Δ ICC where fi = input frequency, CL = output load capacitance, VCC = supply voltage

5.6 Timing Diagrams

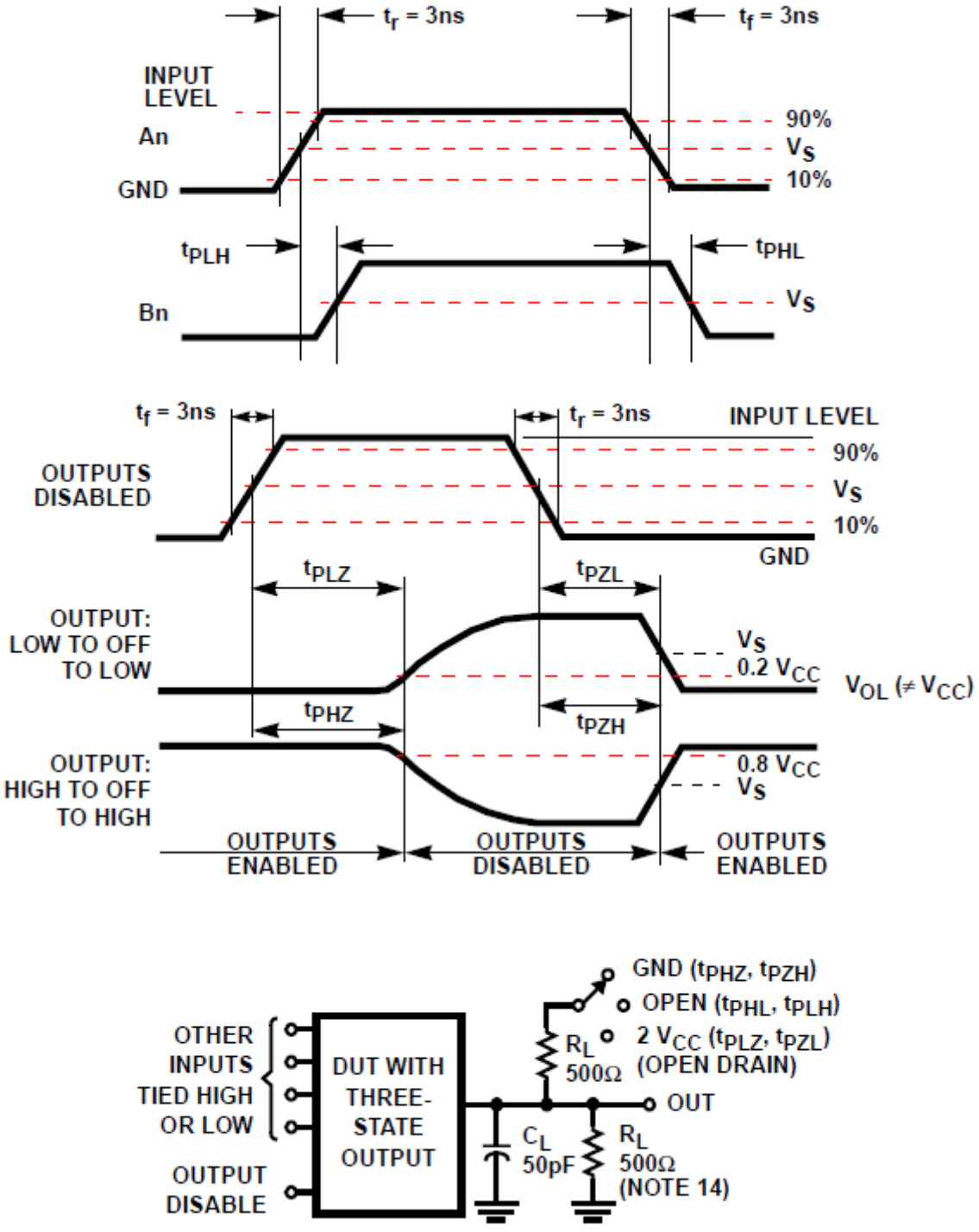


Figure 5-1. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

Figure 5-1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

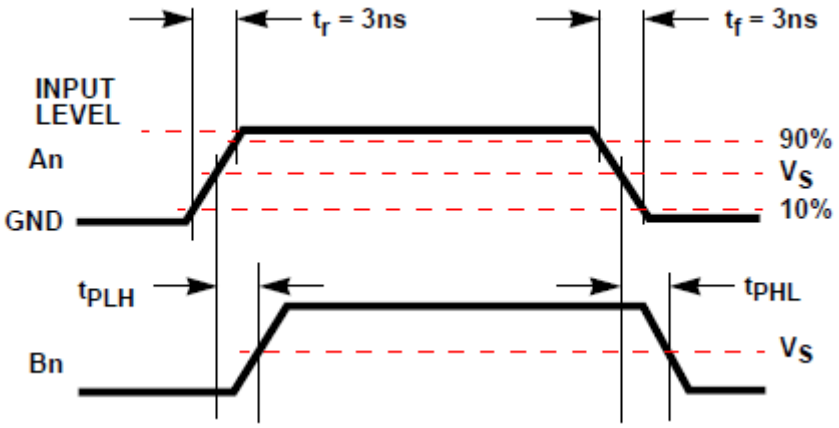
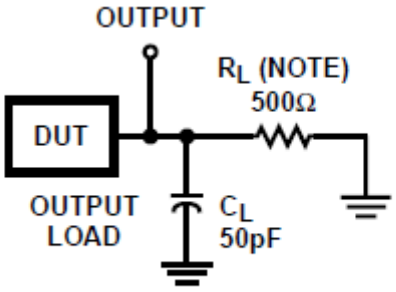


Figure 5-3. PROPAGATION DELAY TIMES



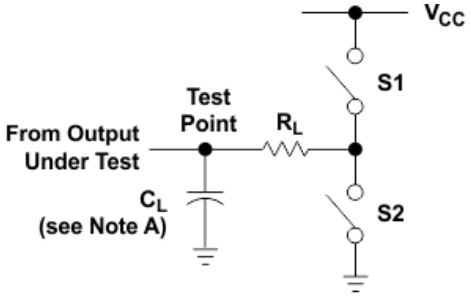
NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

Table 5-1.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

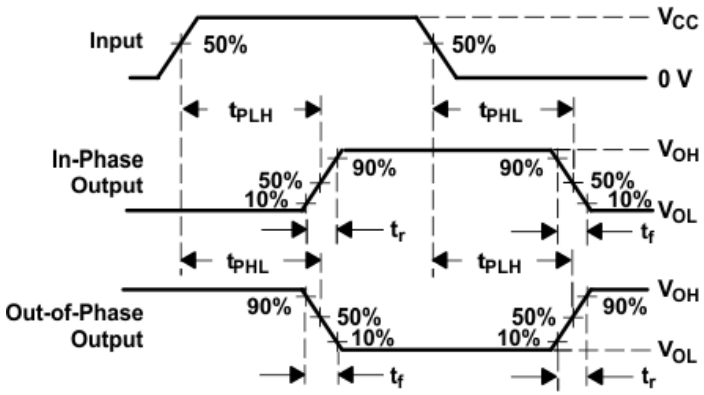
Figure 5-4. PROPAGATION DELAY TIMES

6 Parameter Measurement Information

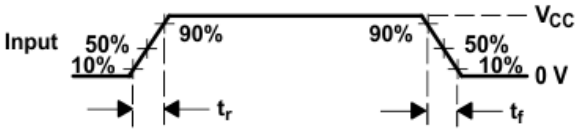


LOAD CIRCUIT

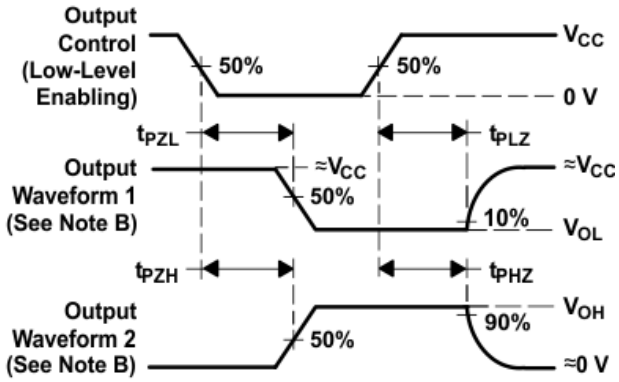
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



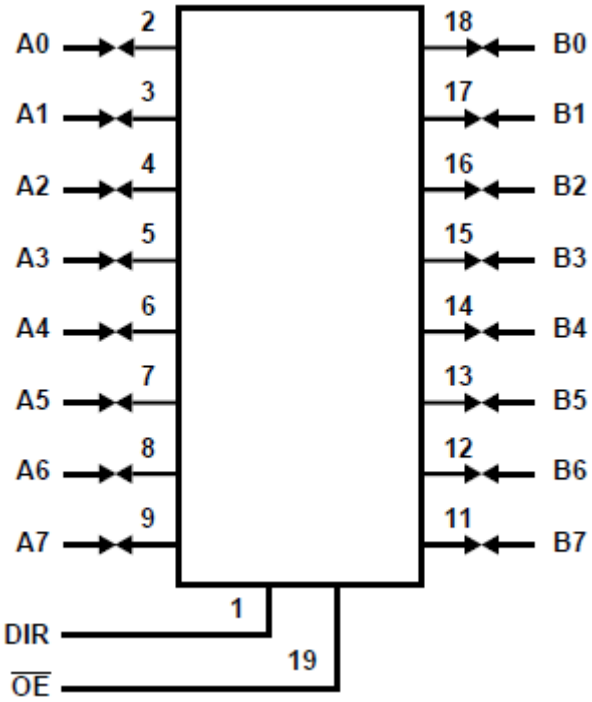
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

7 Detailed Description

7.1 Overview

The 'AC245 and 'ACT245 are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from “A” bus to “B” bus or “B” bus to “A”. The logic level present on the direction input (DIR) determines the data direction. When the output enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Function Table lists the function modes of the CDx4AC245, CDx4ACT245.

Table 7-1. Function Table

INPUTS(1)		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care

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