

## High-Speed CMOS Logic 4-Bit Binary Full Adder with Fast Carry

### 1 Features

- Adds two binary numbers
- Full internal lookahead
- Fast ripple carry for economical expansion
- Operates with both positive and negative logic
- Fanout (over temperature range)
  - Standard outputs 10 LSTTL loads
  - Bus driver outputs 15 LSTTL loads
- Wide operating temperature range:  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V}$  (max),  $V_{IH} = 2\text{ V}$  (min)
  - CMOS input compatibility,  $I_I \leq 1\ \mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

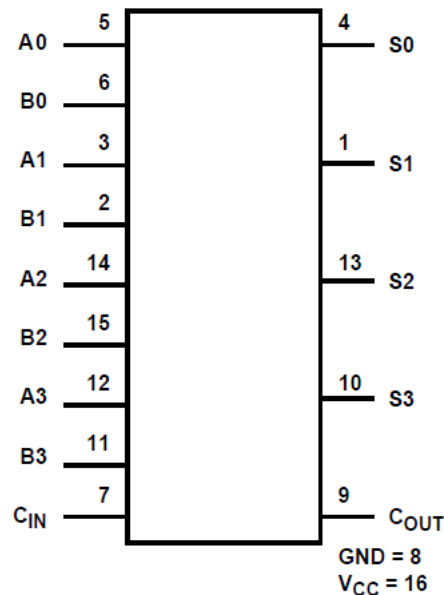
### 2 Description

The CDx4HC283 and CDx4HCT283 contain 4-bit binary adders. The HCT device has TTL-voltage compatible inputs.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD54HC283	J (CDIP, 16)	24.38 mm × 6.92 mm
CD74HC283CD74HC283	D (SOIC, 16)	9.90 mm × 3.90 mm
	N (PDIP, 16)	19.31 mm × 6.35 mm
CD74HCT283CD74HCT283	D (SOIC, 16)	9.90 mm × 3.90 mm
	N (PDIP, 16)	19.31 mm × 6.35 mm

(1) For all packages see the orderable addendum at the end of the datasheet.



Functional Diagram



## Table of Contents

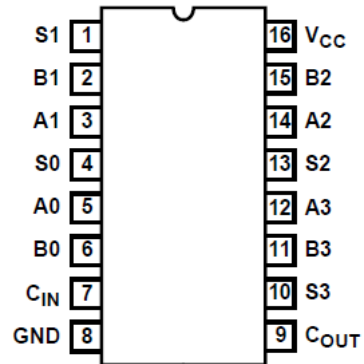
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### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (October 2003) to Revision E (July 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

## 4 Pin Configuration and Functions



J, N, or D package  
16-Pin CDIP, PDIP, or SOIC  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Drain current, per output	For -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25 mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25 mA
Continuous current through V <sub>CC</sub> or GND				±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature range	-65	150	°C
Lead temperature (Soldering 10s)(SOIC - lead tips only)				300 °C

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	2	6	V
V <sub>I</sub> , V <sub>O</sub>	DC input or output voltage	0	V <sub>CC</sub>	V
	Input rise and fall time	2 V	1000	ns
		4.5 V	500	
		6 V	400	
T <sub>A</sub>	Temperature range	-55	125	V

### 5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V <sub>IL</sub>	Low level input voltage		2		0.5		0.5		0.5		V
			4.5		1.35		1.35		1.35		
			6		1.8		1.8		1.8		
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = –20 μA	2	1.9			1.9		1.9		V
		I <sub>OH</sub> = –20 μA	4.5	4.4			4.4		4.4		
		I <sub>OH</sub> = –20 μA	6	5.9			5.9		5.9		
		I <sub>OH</sub> = –4 mA	4.5	3.98			3.84		3.7		V
		I <sub>OH</sub> = –5.2 mA	6	6			5.34		5.2		
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	2		0.1		0.1		0.1		V
		I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1		
		I <sub>OL</sub> = 20 μA	6		0.1		0.1		0.1		
		I <sub>OL</sub> = 4 mA	4.5		0.26		0.33		0.4		V
		I <sub>OL</sub> = 5.2 mA	6		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> or GND	6		±0.1		±1		±1	μA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> or GND	6		8		80		160	μA	
<b>HCT Types</b>											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8		V
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = –20 μA	4.5	4.4			4.4		4.4		V
		I <sub>OH</sub> = –4 mA	4.5	3.98			3.84		3.7		V
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1		V
		I <sub>OL</sub> = 4 mA	4.5		0.26		0.33		0.4		V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> to GND	5.5		±0.1		±1		±1	μA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> or GND	5.5		8		80		160	μA	
ΔI <sub>CC</sub> <sup>(1)</sup>	Additional supply current per input pin	C <sub>IN</sub> input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	540		675		735	μA
		B1, A1, A0 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	360		450		490	μA
		B0 input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	144		180		196	μA
		B3, A3, A2, B2 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	180		225		245	μA

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Switching Characteristics

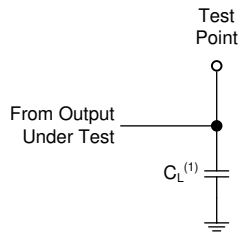
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40 to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay C <sub>IN</sub> to S0	C <sub>L</sub> = 50 pF	2		160		200		240	ns	
			4.5		32		40		45		
		C <sub>L</sub> = 15 pF	5		13						
		C <sub>L</sub> = 50 pF	6		27		34		41		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S1	C <sub>L</sub> = 50 pF	2		180		225		270	ns	
			4.5		36		45		54		
		C <sub>L</sub> = 15 pF	5		15						
		C <sub>L</sub> = 50 pF	6		31		38		46		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S2, C <sub>IN</sub> to C <sub>OUT</sub>	C <sub>L</sub> = 50 pF	2		195		245		295	ns	
			4.5		39		49		59		
		C <sub>L</sub> = 15 pF	5		16						
		C <sub>L</sub> = 50 pF	6		33		42		50		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S3	C <sub>L</sub> = 50 pF	2		230		290		345	ns	
			4.5		46		58		69		
		C <sub>L</sub> = 15 pF	5		19						
		C <sub>L</sub> = 50 pF	6		39		49		59		
t <sub>PLH</sub> , t <sub>PHL</sub>	An, Bn to C <sub>OUT</sub>	C <sub>L</sub> = 50 pF	2		195		245		295	ns	
			4.5		39		49		59		
		C <sub>L</sub> = 15 pF	5		16						
		C <sub>L</sub> = 50 pF	6		33		42		50		
t <sub>PLH</sub> , t <sub>PHL</sub>	An, Bn to Sn	C <sub>L</sub> = 50 pF	2		210		265		315	ns	
			4.5		42		53		63		
		C <sub>L</sub> = 15 pF	5		18						
		C <sub>L</sub> = 50 pF	6		36		45		54		
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time	C <sub>L</sub> = 50 pF	2		75		95		110	ns	
			4.5		15		19		22		
			6		13		16		19		
C <sub>IN</sub>	Input capacitance	C <sub>L</sub> = 50 pF	-		10		10		10	pF	
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>		5		70					pF	
<b>HCT TYPES</b>											
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay C <sub>IN</sub> to S0	C <sub>L</sub> = 15 pF	5		13					ns	
		C <sub>L</sub> = 50 pF	4.5		31		39		47		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S1	C <sub>L</sub> = 15 pF	5		18					ns	
		C <sub>L</sub> = 50 pF	4.5		43		54		65		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S2, C <sub>IN</sub> to C <sub>OUT</sub>	C <sub>L</sub> = 15 pF	5		19					ns	
		C <sub>L</sub> = 50 pF	4.5		46		58		69		
t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>IN</sub> to S3	C <sub>L</sub> = 15 pF	5		22					ns	
		C <sub>L</sub> = 50 pF	4.5		53		66		80		
t <sub>PLH</sub> , t <sub>PHL</sub>	An, Bn to C <sub>OUT</sub>	C <sub>L</sub> = 15 pF	5		20					ns	
		C <sub>L</sub> = 50 pF	4.5		48		60		72		
t <sub>PLH</sub> , t <sub>PHL</sub>	An, Bn to Sn	C <sub>L</sub> = 15 pF	5		21					ns	
		C <sub>L</sub> = 50 pF	4.5		49		61		74		

### 5.5 Switching Characteristics (continued)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			–40 to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time	C <sub>L</sub> = 50 pF	4.5			15		19		22	ns
C <sub>IN</sub>	Input capacitance					10		10		10	pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>		5		82						pF

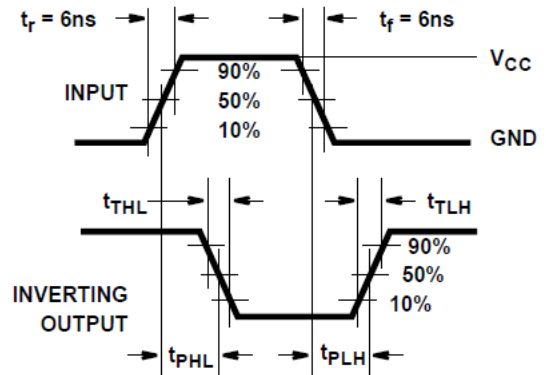
- (1) C<sub>PD</sub> is used to determine the dynamic power consumption, per package.  
 (2) P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where: f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

## 6 Parameter Measurement Information

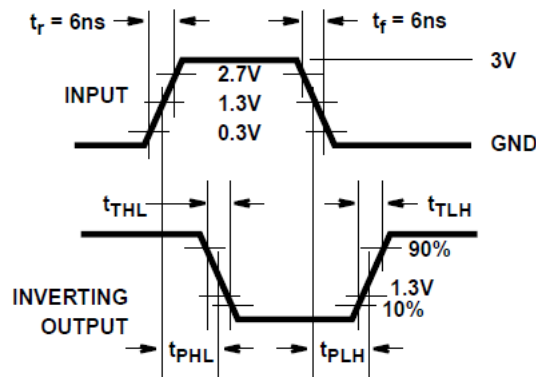


1. Includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Output**



**Figure 6-2. HC and HCT Transition Times and Propagation Delay Times, Combination Logic**



**Figure 6-3. HCT Transition Times and Propagation Delay Times, Combination Logic**

1. The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .
2. The greater between  $t_{plh}$  and  $t_{phl}$  is the same as  $t_{pd}$ .



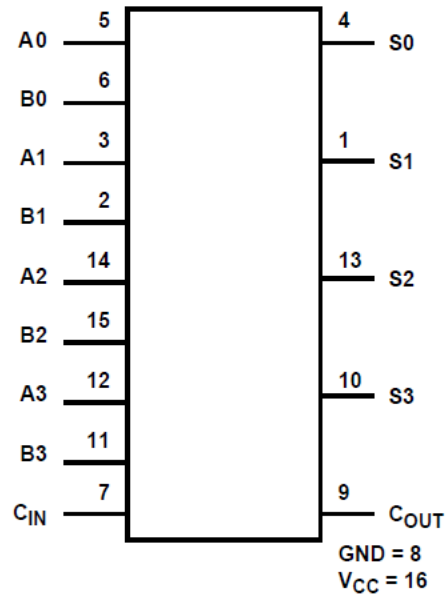
## 7 Detailed Description

### 7.1 Overview

The 'HC283 and 'HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

- Balanced CMOS Push-Pull Outputs
- Clamp Diode Structure

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8976501EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	<a href="#">Samples</a>
CD54HC283F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	<a href="#">Samples</a>
CD54HCT283F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT283F3A	<a href="#">Samples</a>
CD74HC283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC283E	<a href="#">Samples</a>
CD74HC283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M	<a href="#">Samples</a>
CD74HCT283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT283E	<a href="#">Samples</a>
CD74HCT283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HCT283M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC283, CD54HCT283, CD74HC283, CD74HCT283 :**

- Catalog : [CD74HC283](#), [CD74HCT283](#)
- Military : [CD54HC283](#), [CD54HCT283](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC283M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT283M96	SOIC	D	16	2500	366.0	364.0	50.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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