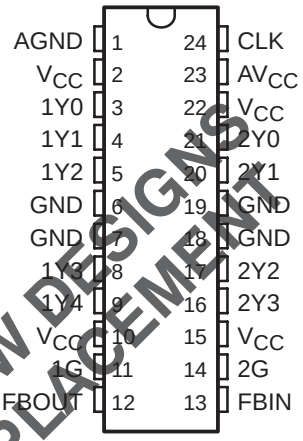
- **Use *CDCVF2509A* as a Replacement for this Device**
- **Designed to Meet PC133 SDRAM Registered DIMM Specification Rev. 0.9**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency 25 MHz to 140 MHz**
- **Static Phase Error Distribution at 66 MHz to 133 MHz is ±125 ps**
- **Jitter (cyc−cyc) at 66 MHz to 133 MHz Is |70| ps**
- **Available in Plastic 24-Pin TSSOP**
- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Terminal Is Used to Synchronize the Outputs to the Clock Input**
- **On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3 V**

PW PACKAGE
(TOP VIEW)



description

The CDCF2509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDCF2509 operates at 3.3 V V_{CC}. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Each bank of outputs is enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDCF2509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDCF2509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

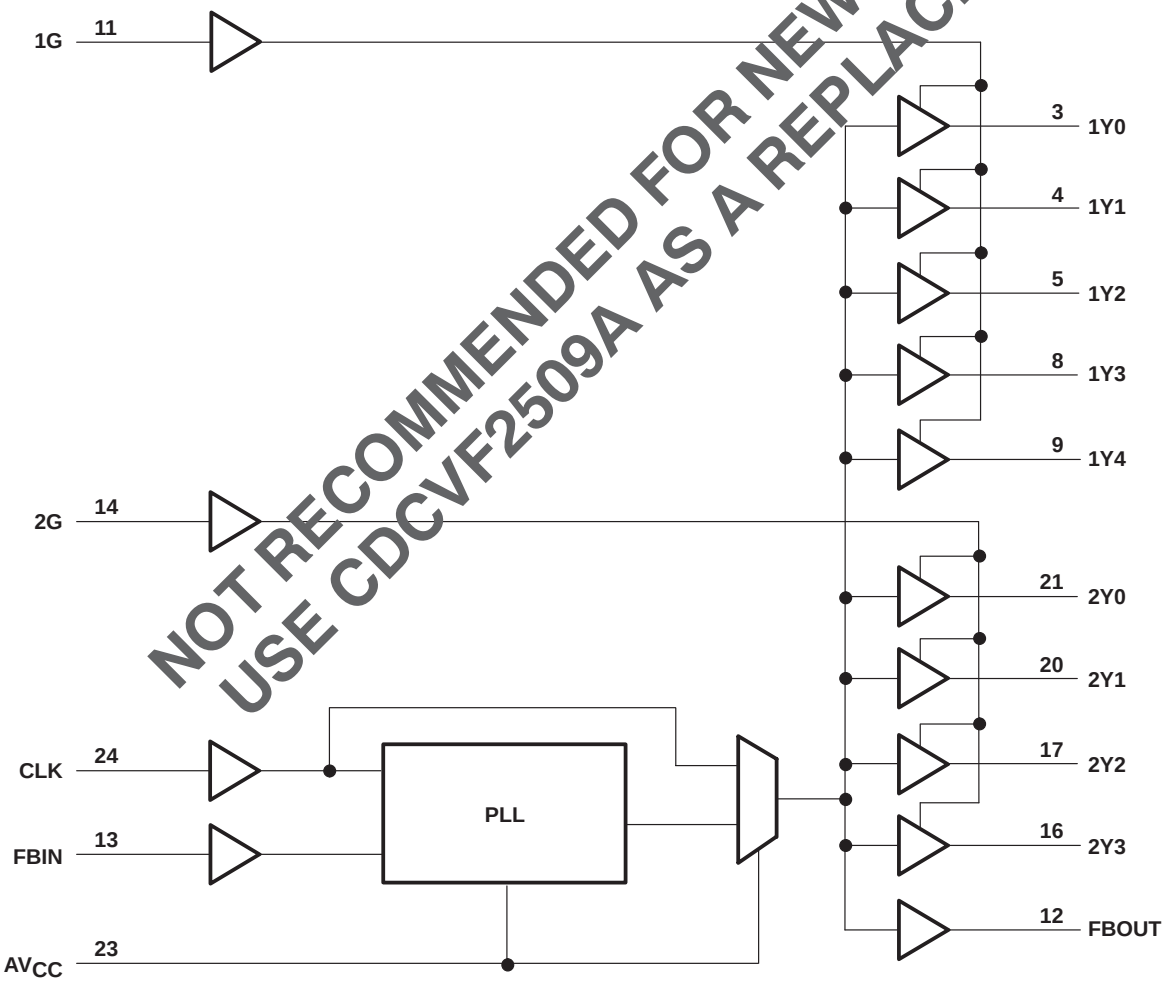
The CDCF2509 is characterized for operation from 0°C to 85°C.

For application information refer to application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (literature number SLMA003) and *Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC)* (literature number SCAA039).

FUNCTION TABLE

INPUTS			OUTPUTS		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 85°C	CDCF2509PWR

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCF2509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switched at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25-Ω series-damping resistor.
2Y (0:3)	21, 20, 17, 16	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{CC} (see Note 1) . . . . . $AV_{CC} < V_{CC}$ +0.7 V
Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 2) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state,
V_O (see Notes 2 and 3) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . . −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 4) . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. AV_{CC} must not exceed V_{CC}.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 4.6 V maximum.
4. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 5)

	MIN	MAX	UNIT
Supply voltage, V_{CC}, AV_{CC}	3	3.6	V
High-level input voltage, V_{IH}	2		V
Low-level input voltage, V_{IL}		0.8	V
Input voltage, V_I	0	V_{CC}	V
High-level output current, I_{OH}		−12	mA
Low-level output current, I_{OL}		12	mA
Operating free-air temperature, T_A	0	85	°C

NOTE 5: Unused inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clk}	Clock frequency	25	140	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time‡		1	ms

‡ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, AV_{CC}	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA	3 V			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −100 µA	MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA	3 V	2.1			
		I_{OH} = −6 mA	3 V	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	3 V			0.8	
		I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current	V_O = 1 V	3.135	−32			
		V_O = 1.65 V	3.3 V		−36		
		V_O = 3.135 V	3.465 V			−12	
I_{OL}	Low-level output current	V_O = 1.95 V	3.135 V	34			
		V_O = 1.65 V	3.3 V		40		
		V_O = 0.4 V	3.465 V			14	
I_I	Input current	V_I = V_{CC} or GND	3.6 V			±5	µA
I_{CC}‡	Supply current	V_I = V_{CC} or GND, I_O = 0, Outputs: low or high	3.6 V			10	µA
ΔI_{CC}	Change in supply current	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3 V		4		pF
C_o	Output capacitance	V_O = V_{CC} or GND	3.3 V		6		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ For I_{CC} of AV_{CC}, and I_{CC} vs Frequency (see Figures 8 and 9).

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF (see Note 6 and Figures 1 and 2)§

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP	MAX	
	Phase error time − static (normalized) (See Figures 3−6)	CLKIN↑ = 66 MHz to133 MHz	FBIN↑	−125		125	ps
$t_{sk(o)}$	Output skew time¶	Any Y or FBOUT	Any Y or FBOUT			200	ps
	Phase error time − jitter (see Note 7)	Clkin = 66 MHz to 100 MHz	Any Y or FBOUT	−50		50	ps
	Jitter$_{(cycle-cycle)}$ (See Figure 7)		Any Y or FBOUT		|70|		
		Clkin = 100 MHz to 133 MHz	Any Y or FBOUT		|65|		
	Duty cycle	F(clkin > 60 MHz)	Any Y or FBOUT	45%		55%	
t_r	Rise time (See Notes 8 and 9)	V_O = 1.2 V to 1.8 V, IBIS simulation	Any Y or FBOUT	2.5		1	V/ns
t_f	Fall time (See Notes 8 and 9)	V_O = 1.2 V to 1.8 V, IBIS simulation	Any Y or FBOUT	2.5		1	V/ns

§ These parameters are not production tested.
¶ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

NOTES: 6. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
7. Calculated per PC DRAM SPEC ($t_{phase\ error}$, static − jitter$_{(cycle-to-cycle)}$).
8. This is equivalent to 0.8 ns/2.5 ns and 0.8 ns/2.7 ns into standard 500 Ω/ 30 pf load for output swing of 0.4 V to 2 V.
9. 64 MB DIMM configuration according to PC SDRAM Registered DIMM Design Support Document, Figure 20 and Table 13.

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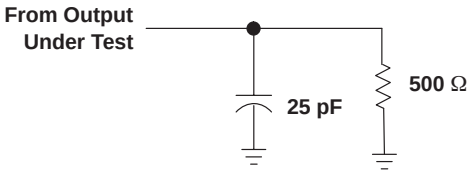
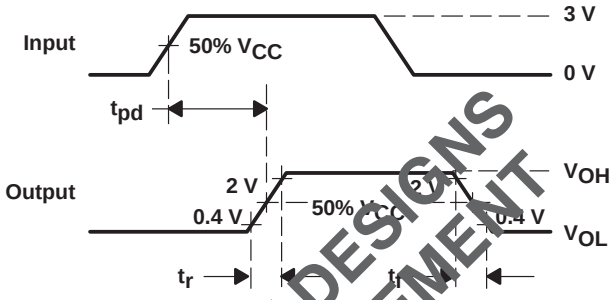
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 133 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

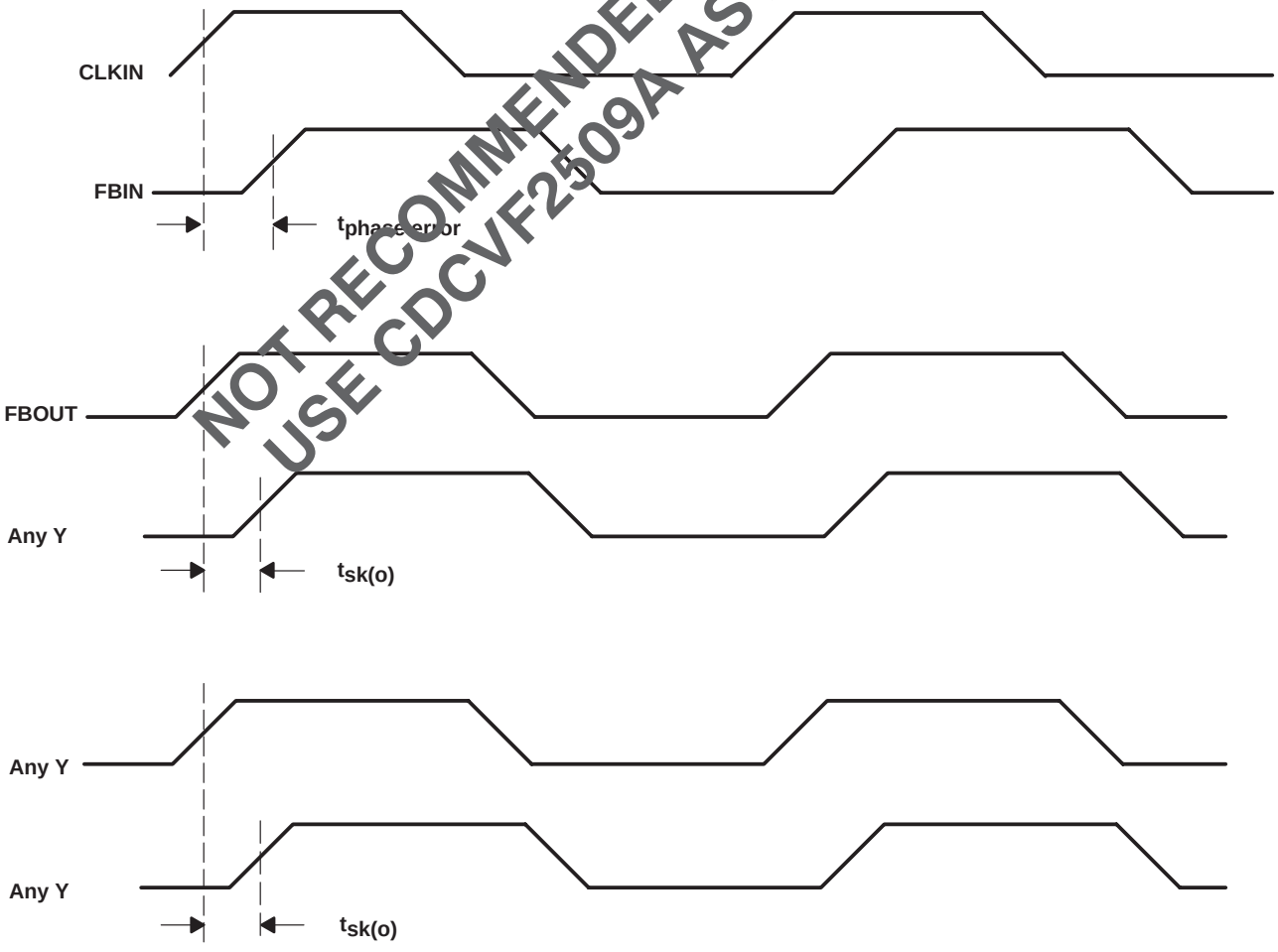


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

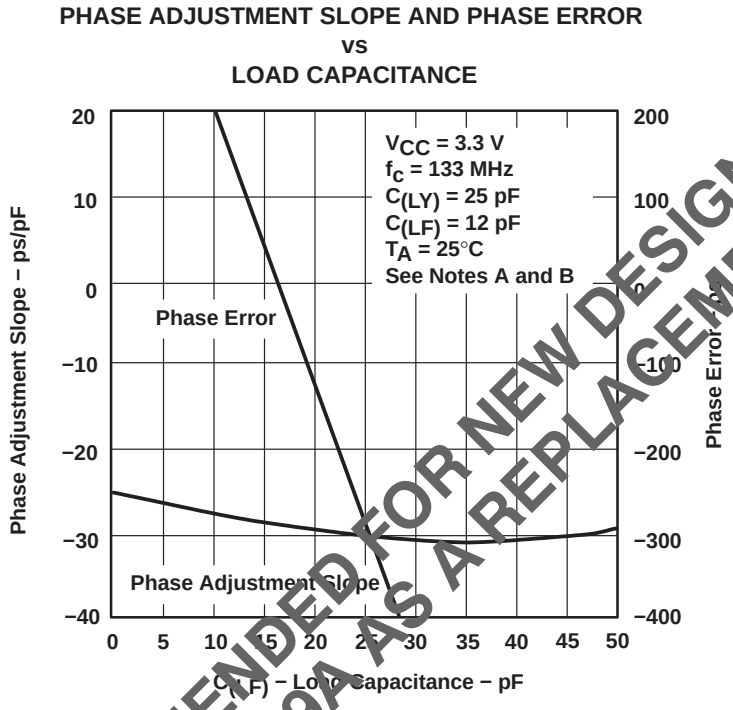


Figure 3

NOTES: A. Trace feedback length FBOUT to FBIN = 5 mm, Z_O = 50 Ω, phase error measured from CLK to Y_n
B. $C_{(LF)}$ = Lumped feedback capacitance at FBIN

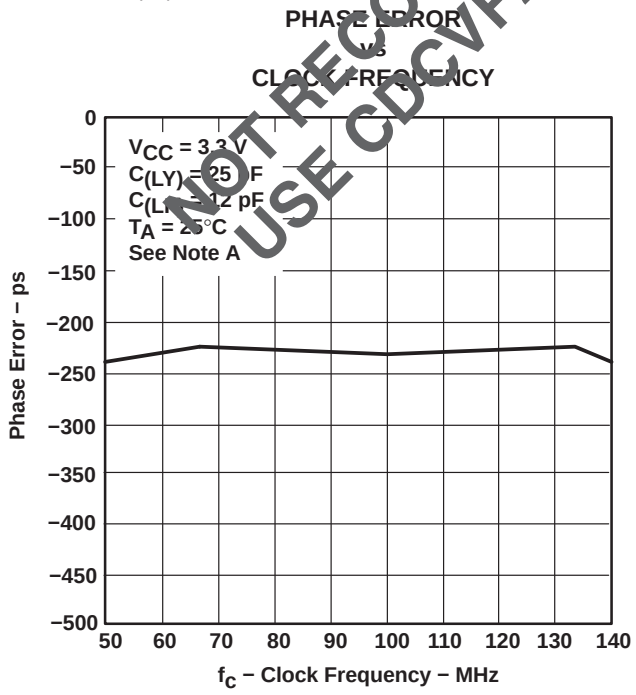


Figure 4

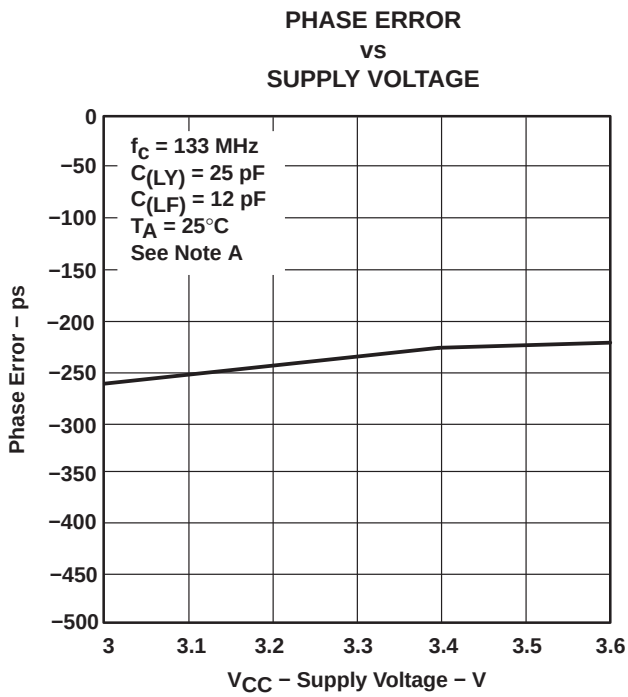


Figure 5

NOTE A: Trace feedback length FBOUT to FBIN = 5 mm, Z_O = 50 Ω

TYPICAL CHARACTERISTICS

STATIC PHASE ERROR vs CLOCK FREQUENCY

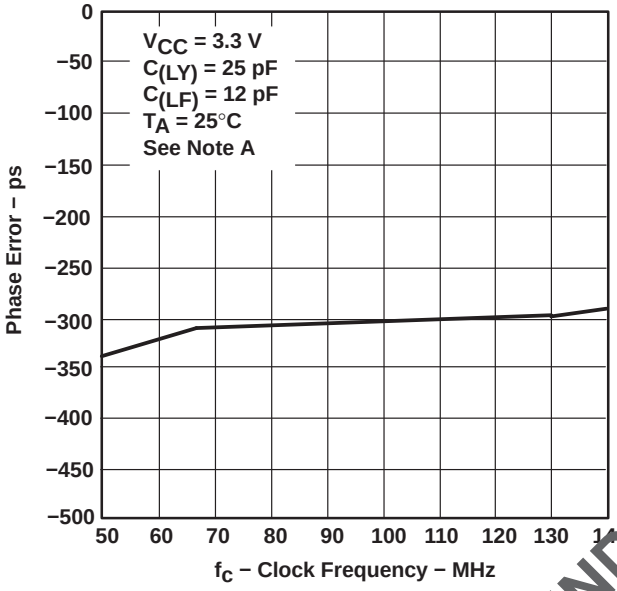


Figure 6

JITTER vs CLOCK FREQUENCY

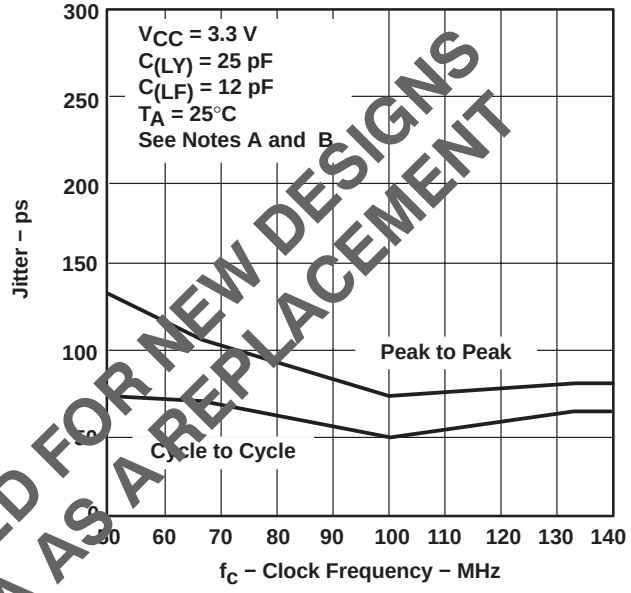


Figure 7

NOTES: A. Trace feedback length FBOUT to FBIN = 5 mm, Z_O = 50 Ω
B. Phase error measured from CLK to FBIN
C. $C_{(LY)}$ = Lumped capacitive load at Y
D. $C_{(LF)}$ = Lumped feedback capacitance at FBIN

ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY

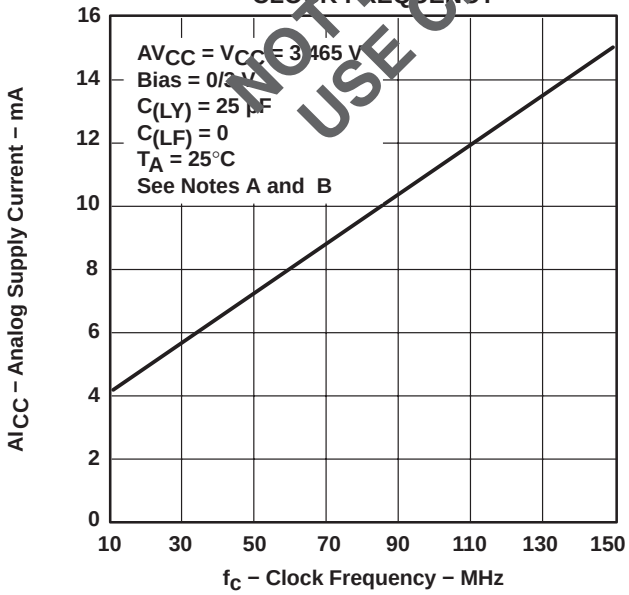


Figure 8

SUPPLY CURRENT vs CLOCK FREQUENCY

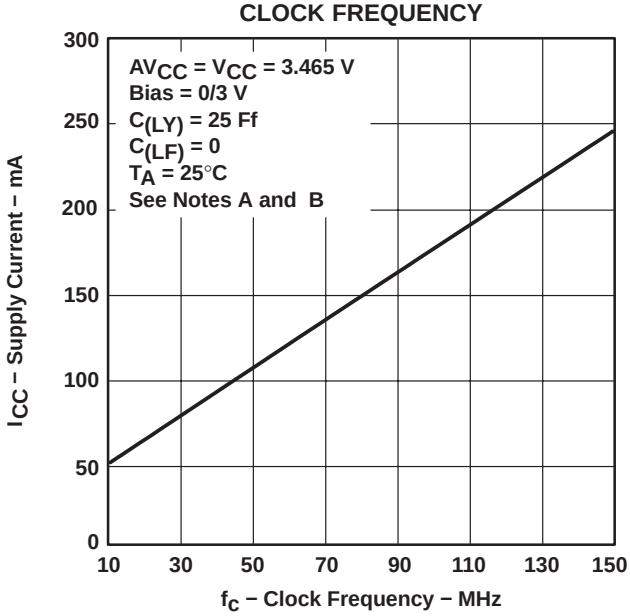


Figure 9

NOTES: A. $C_{(LY)}$ = Lumped capacitive load at Y
B. $C_{(LF)}$ = Lumped feedback capacitance at FBIN

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCF2509PWR	NRND	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDCF2509	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

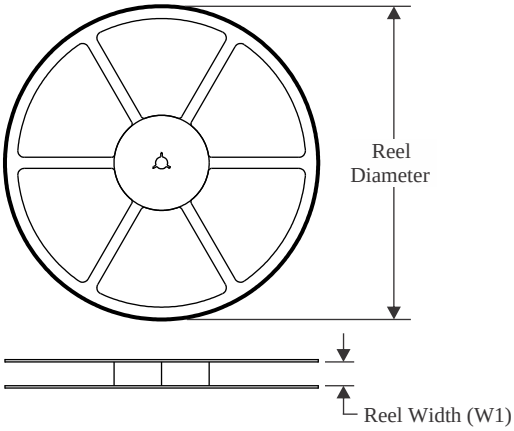
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

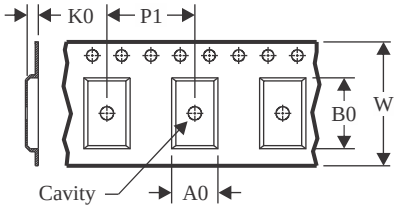
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

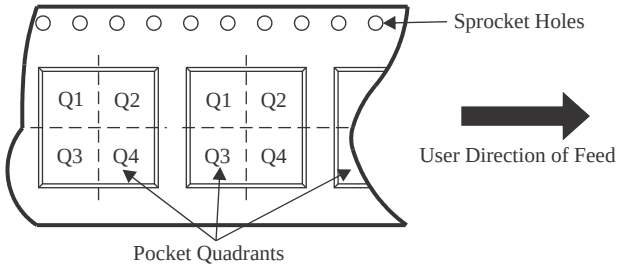


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

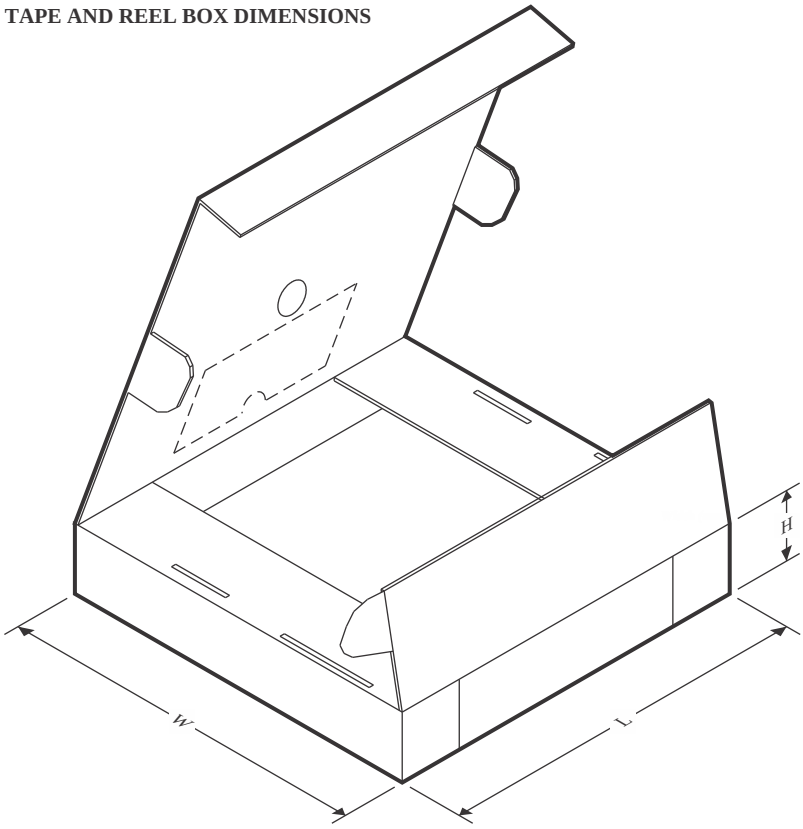
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCF2509PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

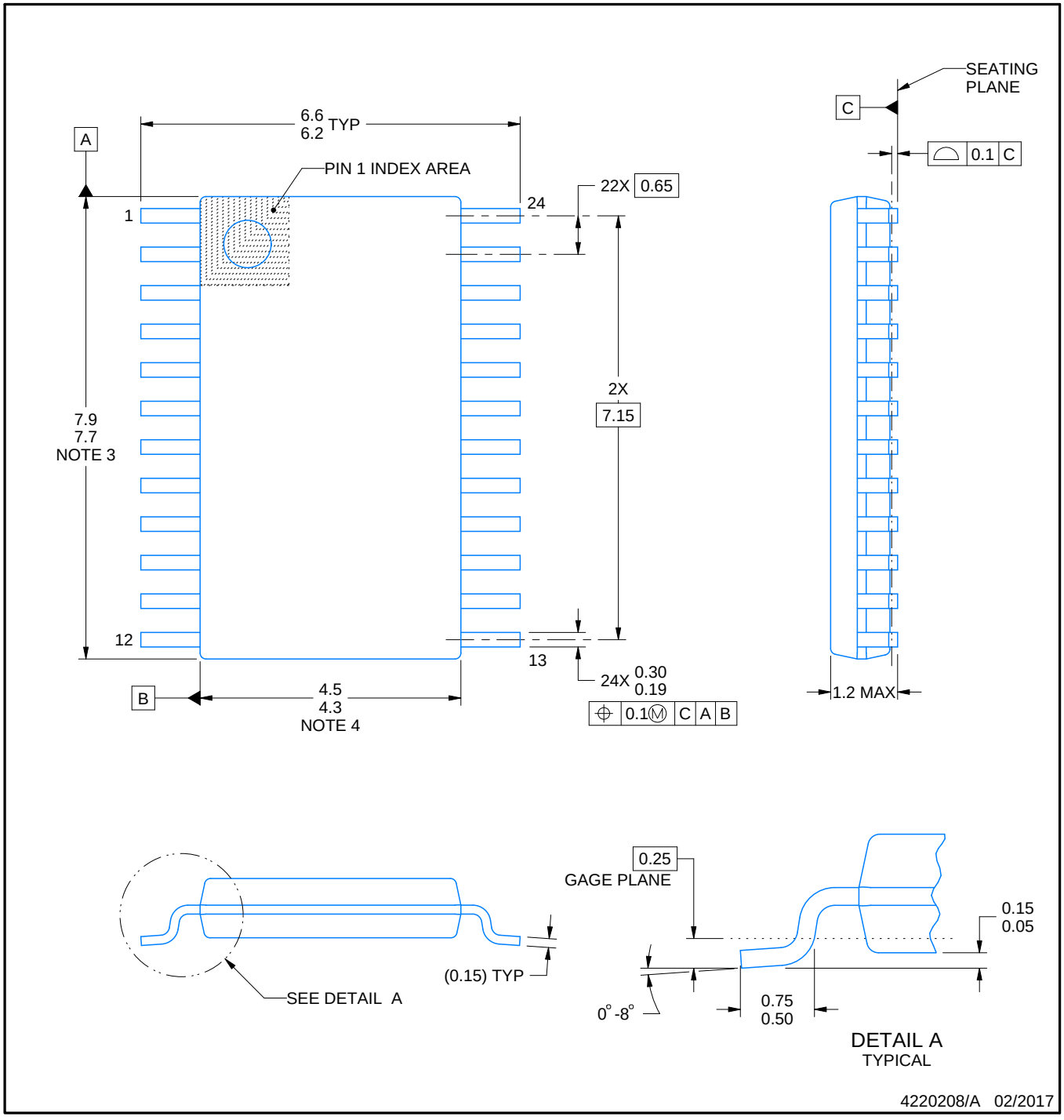
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCF2509PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0024A

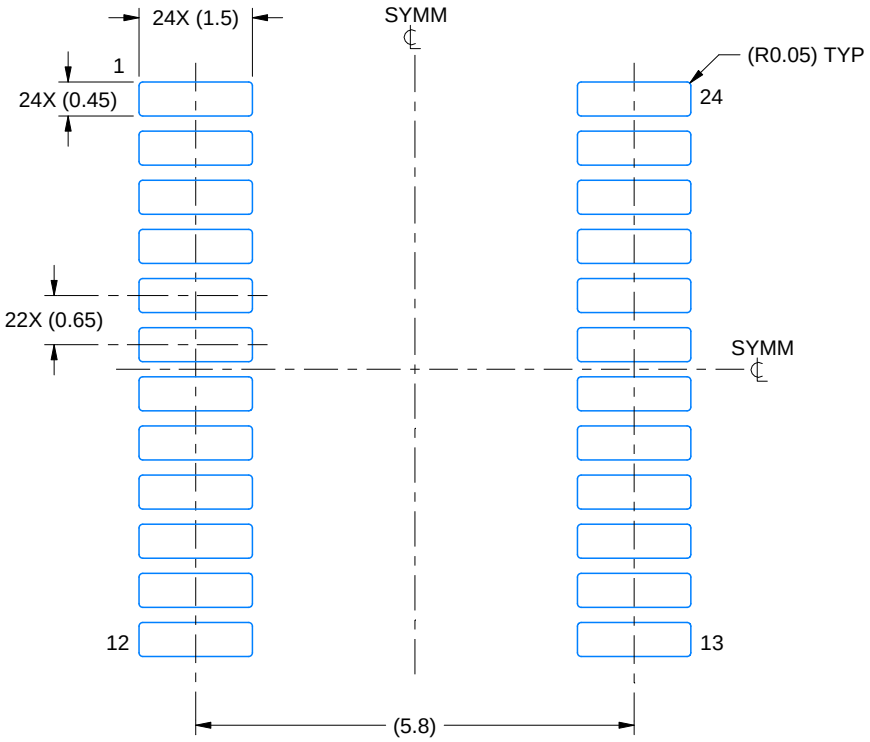
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

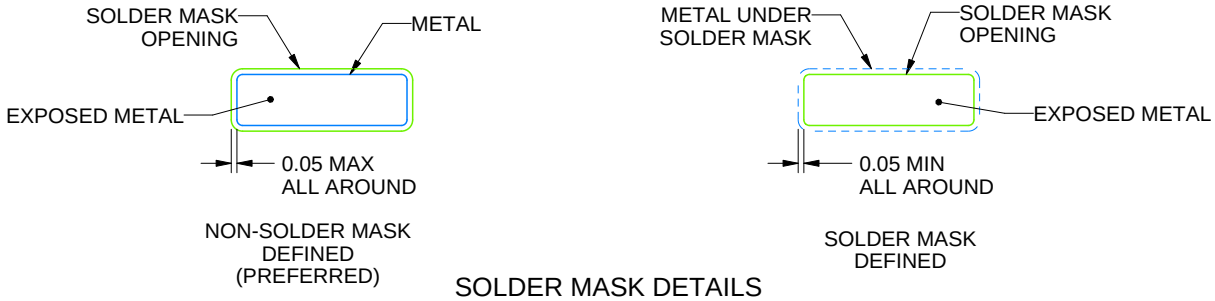


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

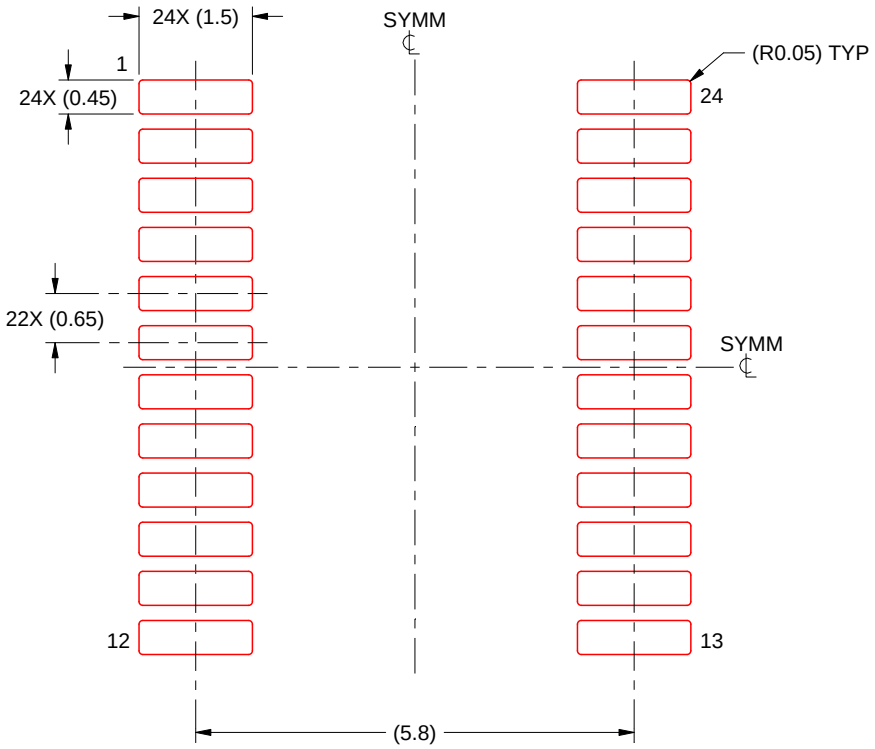


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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