

LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

 Check for Samples: [LF147](#), [LF347-N](#)

FEATURES

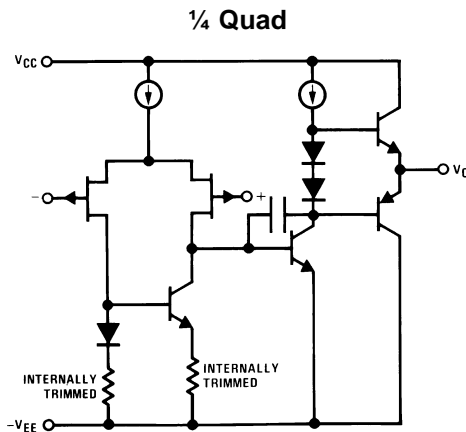
- Internally Trimmed Offset Voltage: 5 mV max
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 7.2 mA
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: $\leq 0.02\%$
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

DESCRIPTION

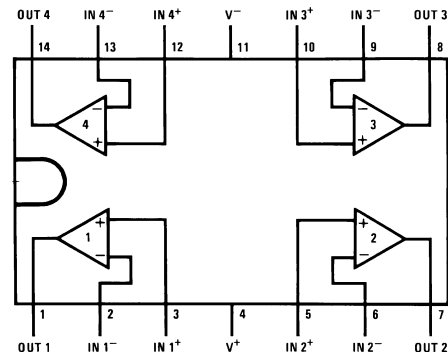
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Simplified Schematic



Connection Diagram



LF147 available as per JM38510/11906.

**Figure 1. 14-Pin PDIP / CDIP / SOIC
Top View
See Package Number J0014A, D0014A or
NFF0014A**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BI-FET II is a trademark of dcl_owner.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

| | | LF147 | LF347B/LF347 |
|--|--------------------|--------------------------------|--------------------|
| Supply Voltage | | ±22V | ±18V |
| Differential Input Voltage | | ±38V | ±30V |
| Input Voltage Range ⁽³⁾ | | ±19V | ±15V |
| Output Short Circuit Duration ⁽⁴⁾ | | Continuous | Continuous |
| Power Dissipation ^{(5) (6)} | | 900 mW | 1000 mW |
| T _j max | | 150°C | 150°C |
| θ _{JA} | CDIP (J) Package | | 70°C/W |
| | PDIP (NFF) Package | | 75°C/W |
| | SOIC Narrow (D) | | 100°C/W |
| | SOIC Wide (D) | | 85°C/W |
| Operating Temperature Range | | See ⁽⁷⁾ | See ⁽⁷⁾ |
| Storage Temperature Range | | -65°C ≤ T _A ≤ 150°C | |
| Lead Temperature (Soldering, 10 sec.) | | 260°C | 260°C |
| Soldering Information | PDIP / CDIP | Soldering (10 seconds) | 260°C |
| | SOIC Package | Vapor Phase (60 seconds) | 215°C |
| | | Infrared (15 seconds) | 220°C |
| ESD Tolerance ⁽⁸⁾ | | | 900V |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- (4) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (5) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA}.
- (6) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside ensured limits.
- (7) The LF147 is available in the military temperature range -55°C ≤ T_A ≤ 125°C, while the LF347B and the LF347 are available in the commercial temperature range 0°C ≤ T_A ≤ 70°C. Junction temperature can rise to T_j max = 150°C.
- (8) Human body model, 1.5 kΩ in series with 100 pF.

DC Electrical Characteristics ⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|----------------------|------------------------------------|---|-------|------------------|-----|--------|------------------|-----|-------|------------------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S =10 kΩ, T _A =25°C | | 1 | 5 | | 3 | 5 | | 5 | 10 | mV |
| | | Over Temperature | | | 8 | | 7 | | | | 13 | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S =10 kΩ | | 10 | | | 10 | | | 10 | | μV/°C |
| I _{OS} | Input Offset Current | T _j =25°C, ^{(2) (3)} | | 25 | 100 | | 25 | 100 | | 25 | 100 | pA |
| | | Over Temperature | | | 25 | | 4 | | | | 4 | nA |
| I _B | Input Bias Current | T _j =25°C, ^{(2) (3)} | | 50 | 200 | | 50 | 200 | | 50 | 200 | pA |
| | | Over Temperature | | | 50 | | 8 | | | | 8 | nA |
| R _{IN} | Input Resistance | T _j =25°C | | 10 ¹² | | | 10 ¹² | | | 10 ¹² | | Ω |

- (1) Refer to RETS147X for LF147D and LF147J military specifications.
- (2) Unless otherwise specified the specifications apply over the full temperature range and for V_S=±20V for the LF147 and for V_S=±15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.
- (3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{JA} P_D where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

DC Electrical Characteristics ⁽¹⁾⁽²⁾ (continued)

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|------------------|---------------------------------|--|-------|-------|-----|--------|-------|-----|-------|-------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| A _{VOL} | Large Signal Voltage Gain | V _S =±15V, T _A =25°C V _O =±10V, R _L =2 kΩ Over Temperature | 50 | 100 | | 50 | 100 | | 25 | 100 | | V/mV |
| | | | 25 | | | 25 | | | 15 | | | V/mV |
| V _O | Output Voltage Swing | V _S =±15V, R _L =10 kΩ | ±12 | ±13.5 | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| V _{CM} | Input Common-Mode Voltage Range | V _S =±15V | ±11 | +15 | | ±11 | +15 | | ±11 | +15 | | V |
| | | | | -12 | | | -12 | | | -12 | | V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤10 kΩ | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | See ⁽⁴⁾ | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| I _S | Supply Current | | | 7.2 | 11 | | 7.2 | 11 | | 7.2 | 11 | mA |

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ± 5V to ±15V for the LF347 and LF347B and from V_S = ±20V to ±5V for the LF147.

AC Electrical Characteristics ⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|----------------|---------------------------------|--|-------|-------|-----|--------|-------|-----|-------|-------|-----|----------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | T _A =25°C, f=1 Hz-20 kHz (Input Referred) | | -120 | | | -120 | | | -120 | | dB |
| SR | Slew Rate | V _S =±15V, T _A =25°C | 8 | 13 | | 8 | 13 | | 8 | 13 | | V/μs |
| GBW | Gain-Bandwidth Product | V _S =±15V, T _A =25°C | 2.2 | 4 | | 2.2 | 4 | | 2.2 | 4 | | MHz |
| e _n | Equivalent Input Noise Voltage | T _A =25°C, R _S =100Ω, f=1000 Hz | | 20 | | | 20 | | | 20 | | nV / √Hz |
| i _n | Equivalent Input Noise Current | T _J =25°C, f=1000 Hz | | 0.01 | | | 0.01 | | | 0.01 | | pA / √Hz |
| THD | Total Harmonic Distortion | A _V =+10, R _L =10k, V _O =20 Vp-p, BW=20 Hz-20 kHz | | <0.02 | | | <0.02 | | | <0.02 | | % |

(1) Unless otherwise specified the specifications apply over the full temperature range and for V_S=±20V for the LF147 and for V_S=±15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

(2) Refer to RETS147X for LF147D and LF147J military specifications.

Typical Performance Characteristics

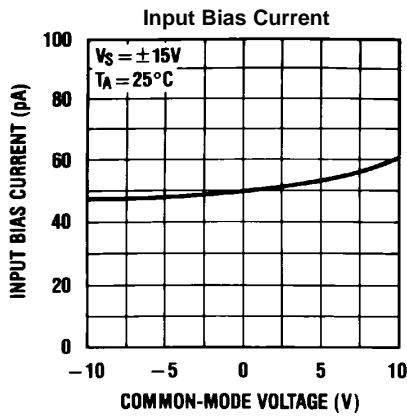


Figure 2.

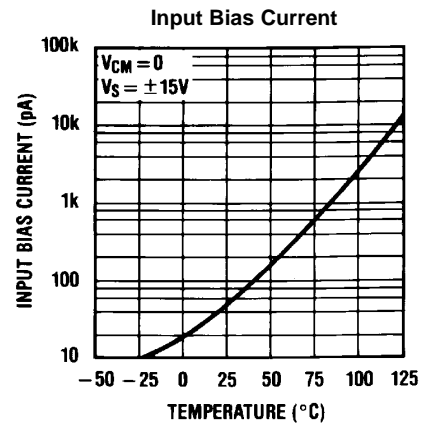


Figure 3.

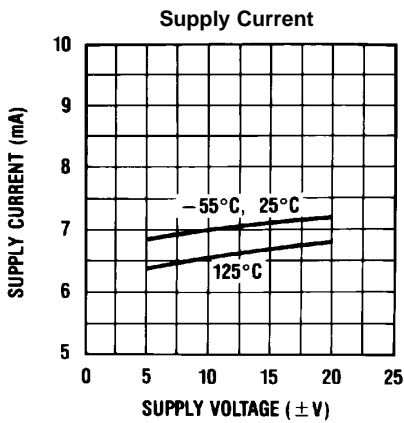


Figure 4.

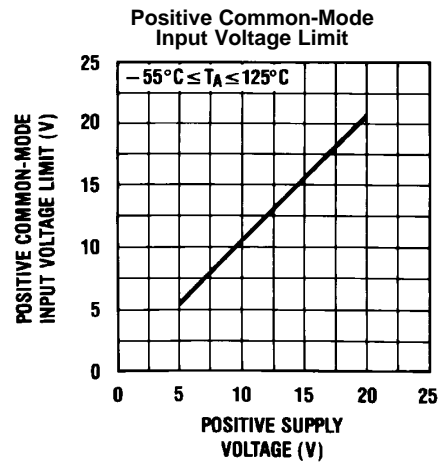


Figure 5.

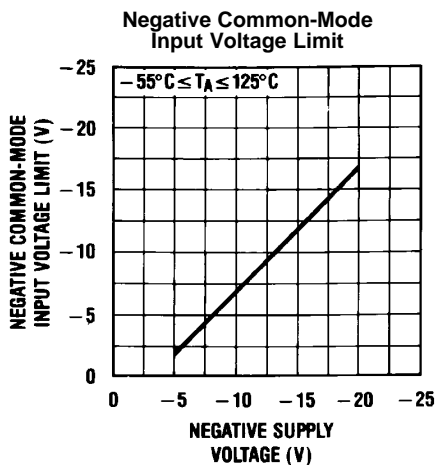


Figure 6.

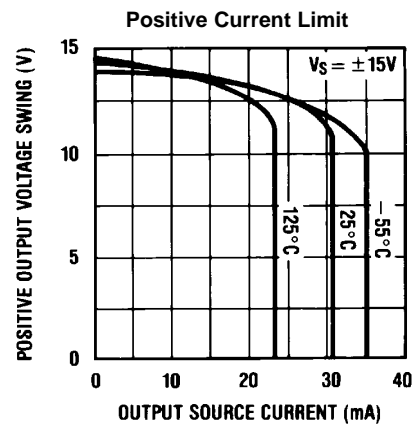


Figure 7.

Typical Performance Characteristics (continued)

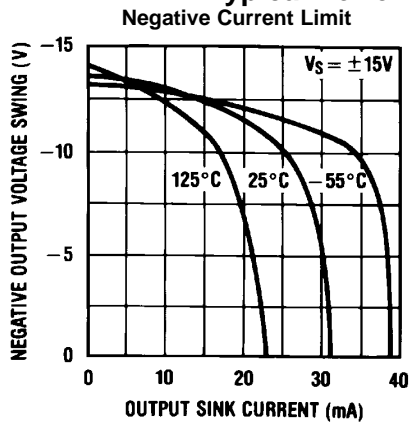


Figure 8.

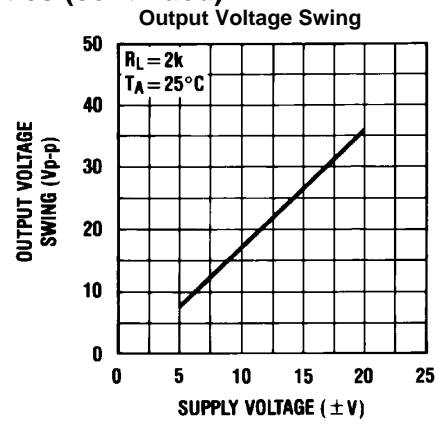


Figure 9.

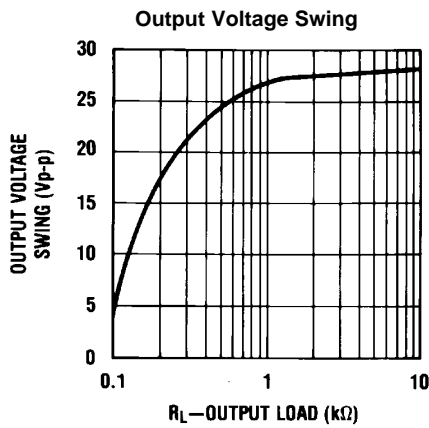


Figure 10.

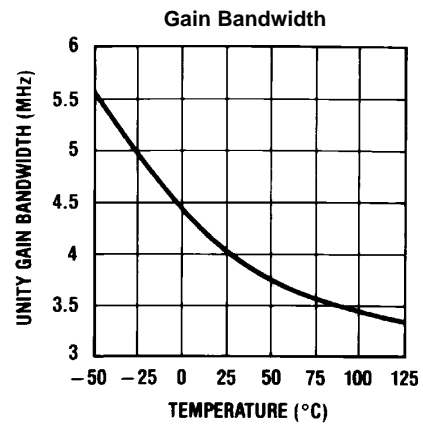


Figure 11.

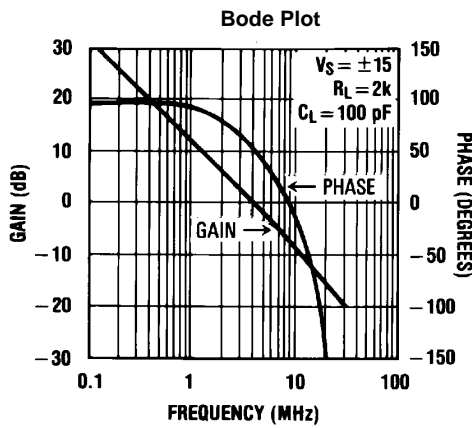


Figure 12.

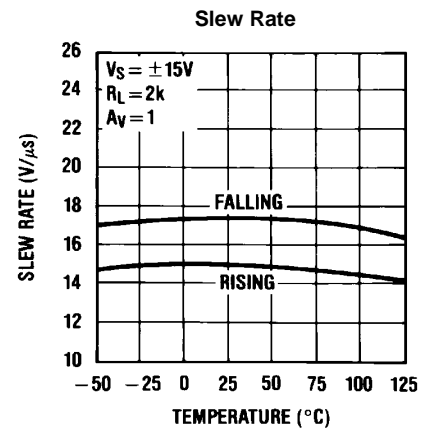
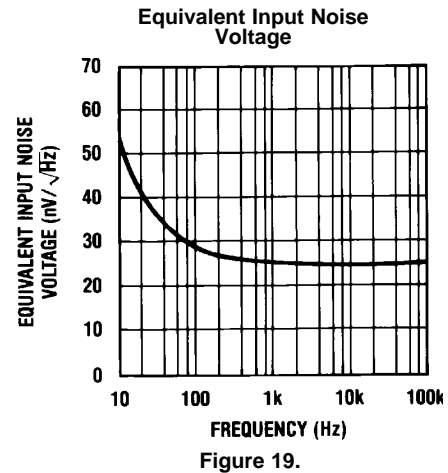
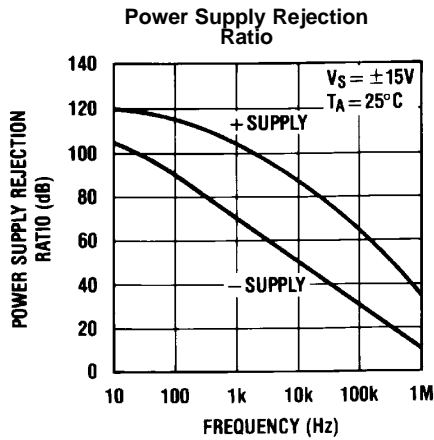
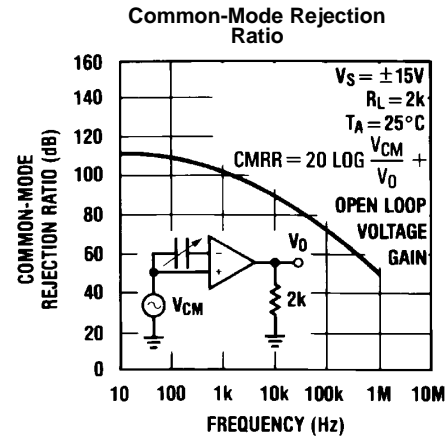
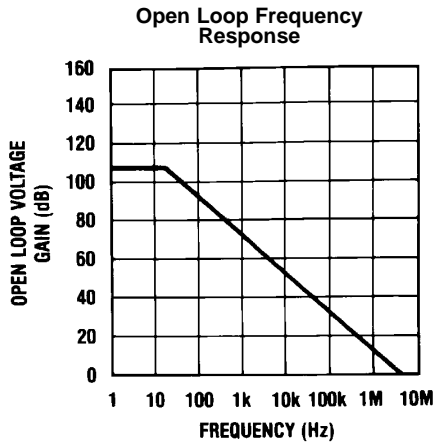
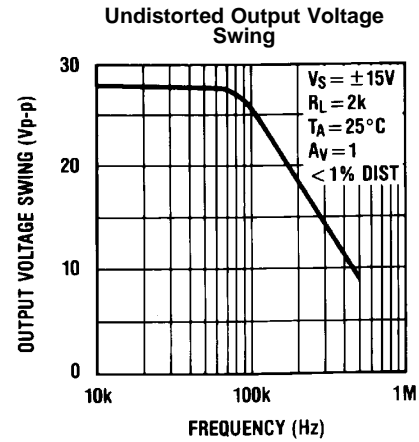
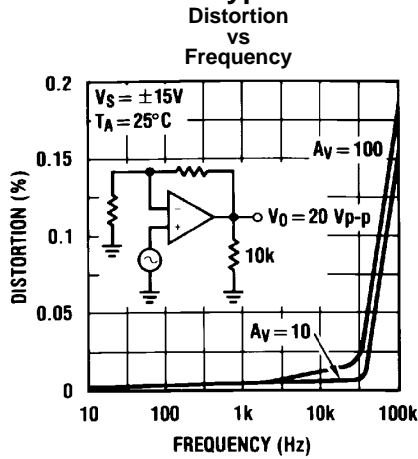
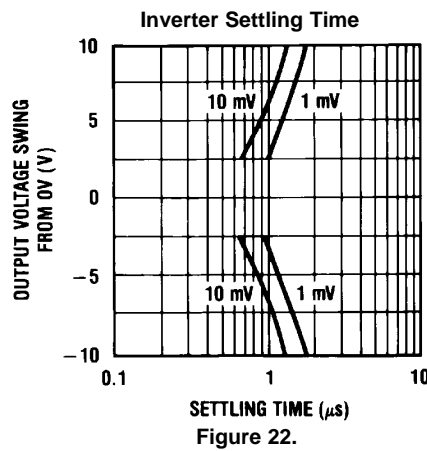
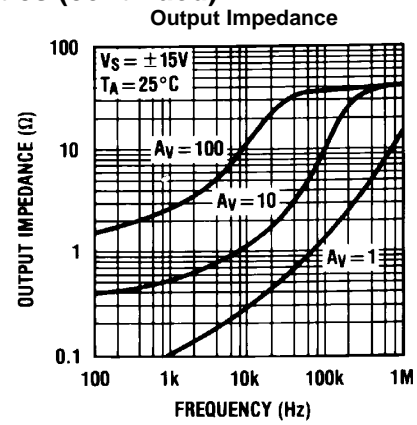
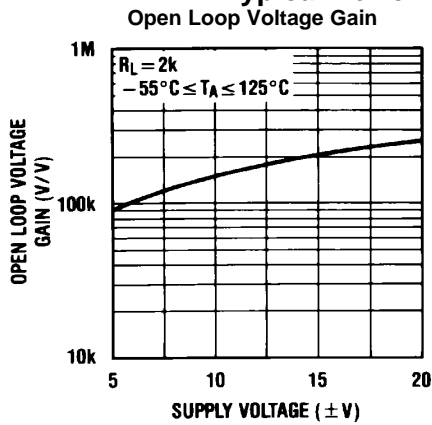


Figure 13.

Typical Performance Characteristics (continued)



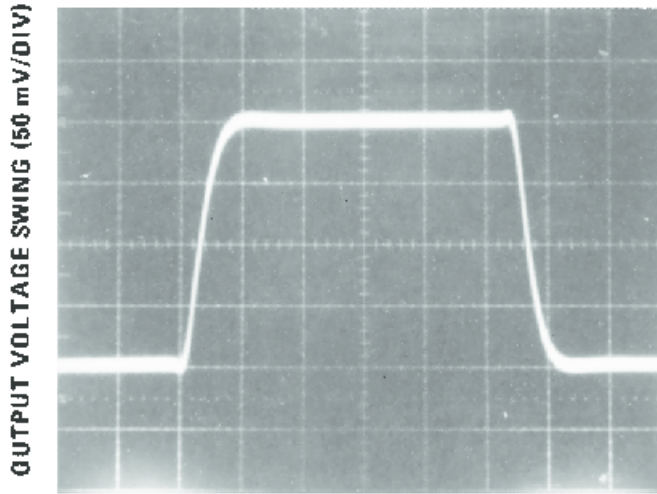
Typical Performance Characteristics (continued)



Pulse Response

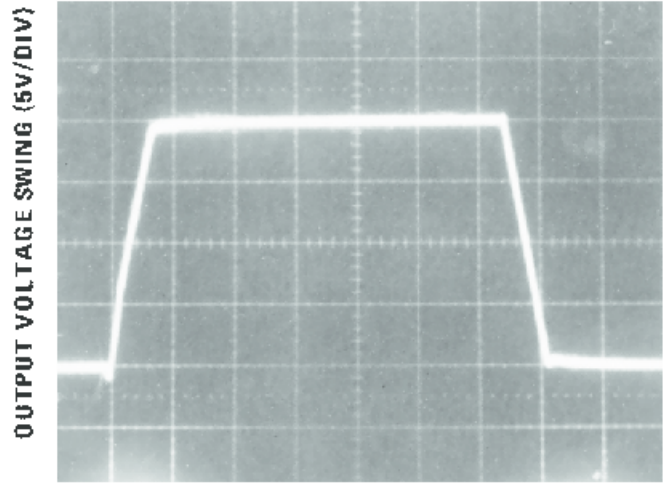
$R_L=2\text{ k}\Omega$, $C_L=10\text{ pF}$

Small Signal Inverting



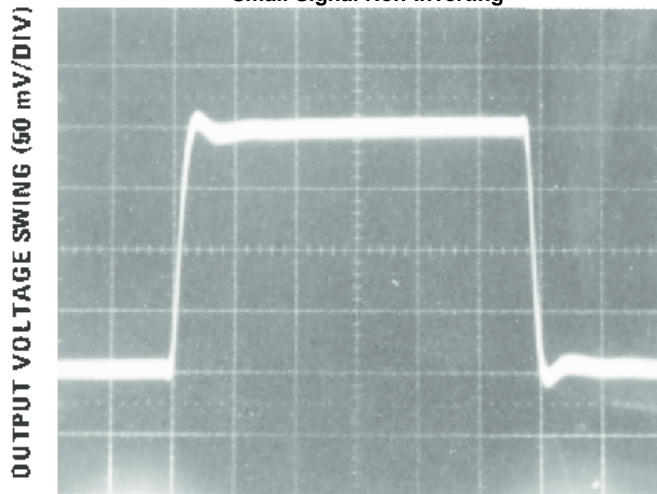
TIME (0.2 $\mu\text{s/DIV}$)

Large Signal Inverting



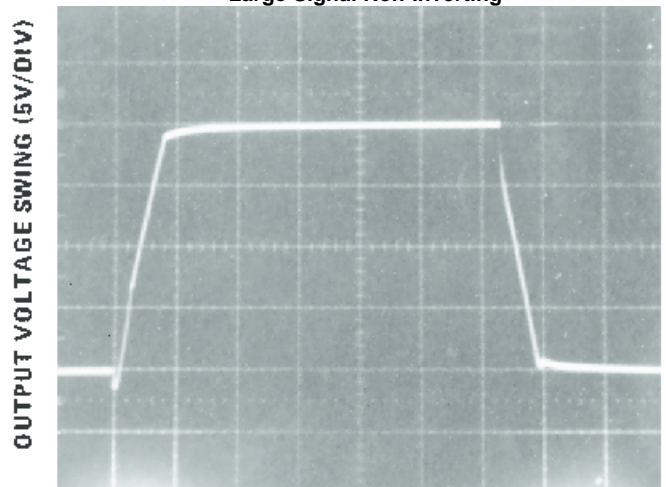
TIME (2 $\mu\text{s/DIV}$)

Small Signal Non-Inverting



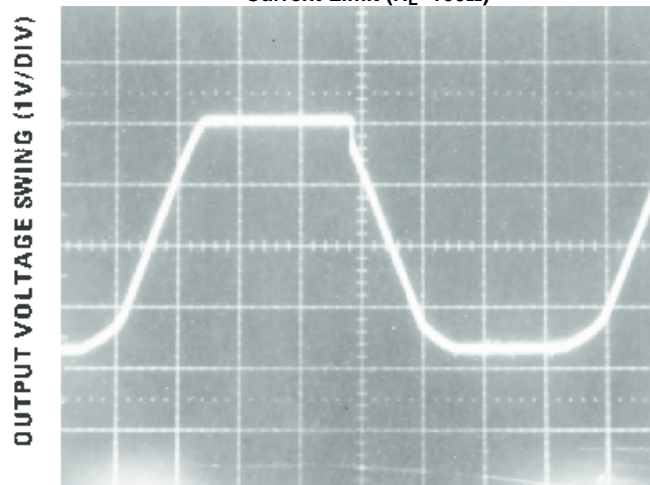
TIME (0.2 $\mu\text{s/DIV}$)

Large Signal Non-Inverting



TIME (2 $\mu\text{s/DIV}$)

Current Limit ($R_L=100\Omega$)



TIME (5 $\mu\text{s/DIV}$)

APPLICATION HINTS

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 4.5\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

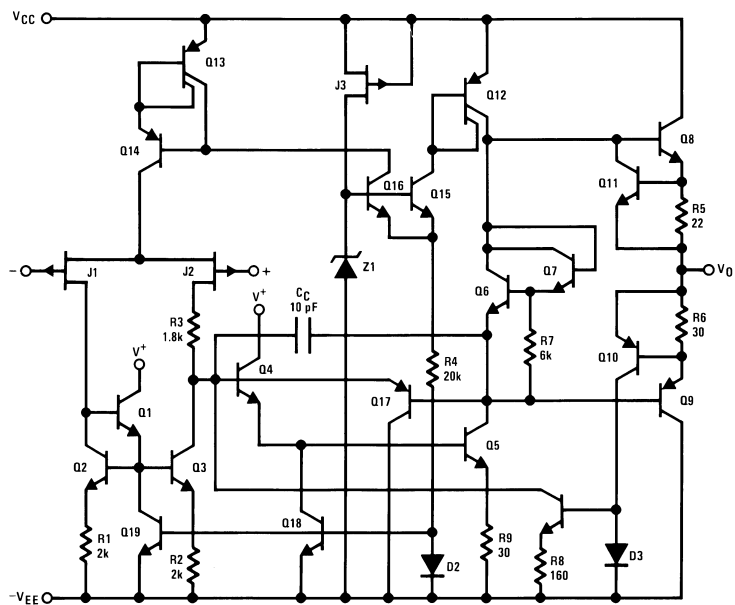
The LF147 will drive a 2 k Ω load resistance to $\pm 10\text{V}$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

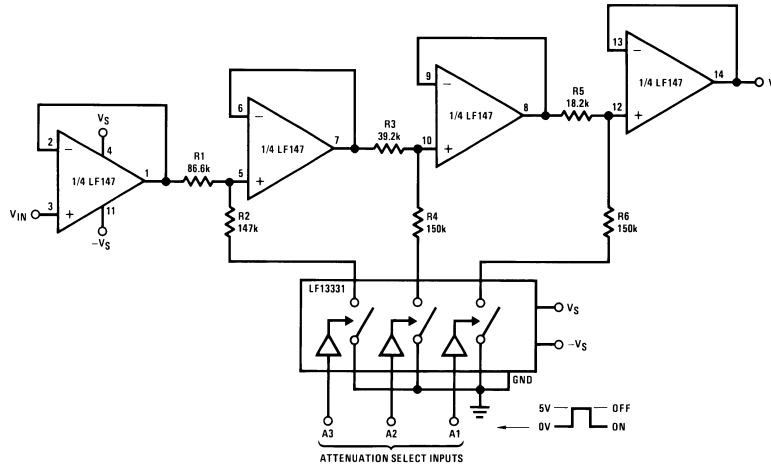
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Figure 23. Digitally Selectable Precision Attenuator

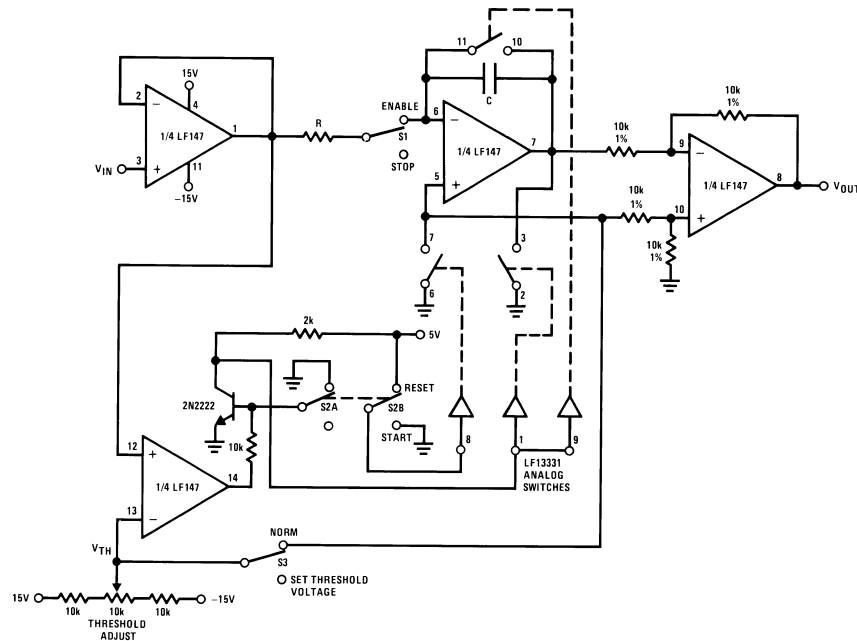


All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

| A1 | A2 | A3 | V _O Attenuation |
|----|----|----|-------------------------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | -1 dB |
| 0 | 1 | 0 | -2 dB |
| 0 | 1 | 1 | -3 dB |
| 1 | 0 | 0 | -4 dB |
| 1 | 0 | 1 | -5 dB |
| 1 | 1 | 0 | -6 dB |
| 1 | 1 | 1 | -7 dB |

Figure 24. Long Time Integrator with Reset, Hold and Starting Threshold Adjustment

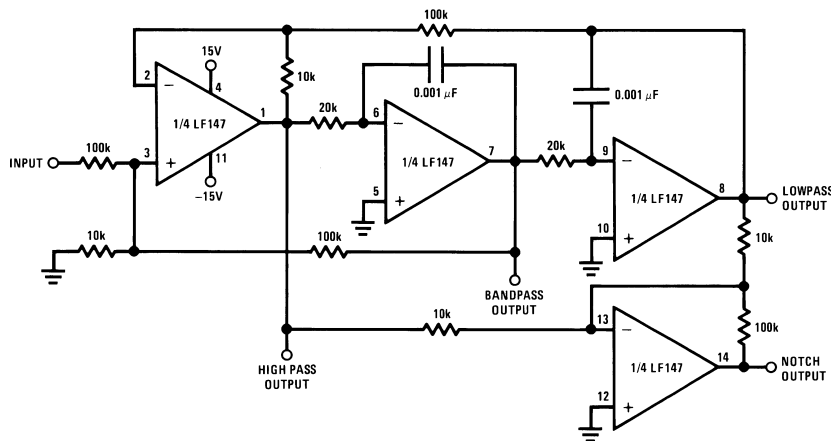


- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Figure 25. Universal State Variable Filter



For circuit shown:

$f_0 = 3 \text{ kHz}$, $f_{NOTCH} = 9.5 \text{ kHz}$

$Q = 3.4$

Passband gain:

Highpass—0.1

Bandpass—1

Lowpass—1

Notch—10

- $f_0 \times Q \leq 200 \text{ kHz}$
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|--|--------------------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 12 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LF147-MD8 | ACTIVE | DIE SALE | Y | 0 | 100 | RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | | Samples |
| LF147J | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LF147J | Samples |
| LF347BN/NOPB | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | 0 to 70 | LF347BN | Samples |
| LF347M | LIFEBUY | SOIC | D | 14 | 55 | Non-RoHS & Green | Call TI | Level-1-235C-UNLIM | 0 to 70 | LF347M | |
| LF347M/NOPB | ACTIVE | SOIC | D | 14 | 55 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LF347M | Samples |
| LF347MX | LIFEBUY | SOIC | D | 14 | 2500 | Non-RoHS & Green | Call TI | Level-1-235C-UNLIM | 0 to 70 | LF347M | |
| LF347MX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LF347M | Samples |
| LF347N/NOPB | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | 0 to 70 | LF347N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LF347MX | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LF347MX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LF347MX | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LF347MX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LF147J | J | CDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |
| LF347BN/NOPB | N | PDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |
| LF347M | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LF347M | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LF347M/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LF347N/NOPB | N | PDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

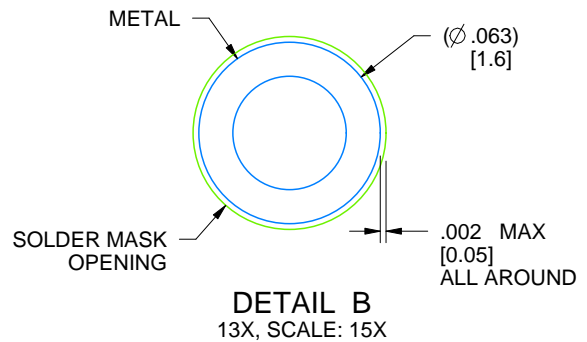
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



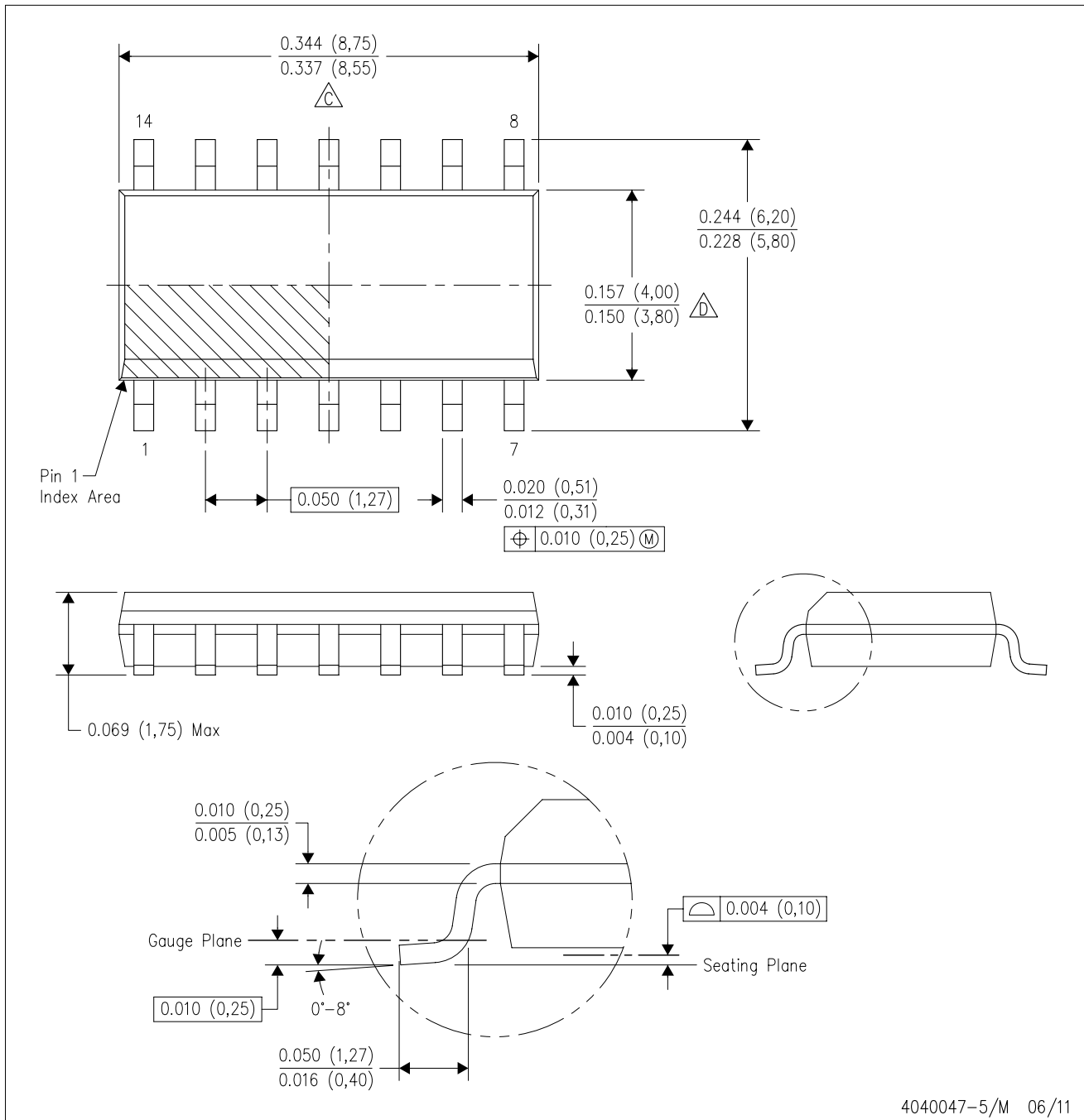
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated