LMH6738 Very Wideband, Low Distortion Triple Op Amp

Check for Samples: LMH6738

FEATURES

- **750 MHz −3 dB small signal bandwidth (A_V = +1)**
- **−85 dBc 3rd harmonic distortion (20 MHz)**
- **2.3 nV/$\overline{Hz}$ input noise voltage**
- **3300 V/µs slew rate**
- **33 mA supply current (11.3 mA per op amp)**
- **90 mA linear output current**
- **0.02/0.01 Diff. Gain / Diff. Phase (R_L = 150Ω)**

APPLICATIONS

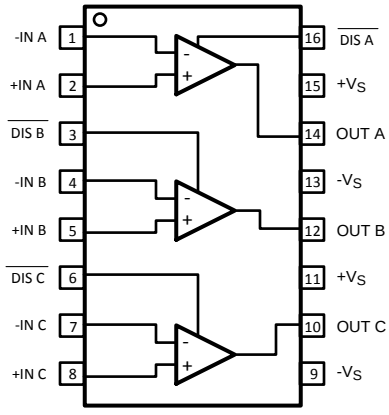
- **RGB video driver**
- **High resolution projectors**
- **Flash A/D driver**
- **D/A transimpedance buffer**
- **Wide dynamic range IF amp**
- **Radar/communication receivers**
- **DDS post-amps**
- **Wideband inverting summer**
- **Line driver**

DESCRIPTION

The LMH6738 is a very wideband, DC coupled monolithic operational amplifier designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from TI's current feedback architecture, the LMH6738 offers a gain range of ±1 to ±10 while providing stable, operation without external compensation, even at unity gain. At a gain of +2 the LMH6738 supports ultra high resolution video systems with a 400 MHz 2 V_{PP} –3 dB Bandwidth. With 12-bit distortion levels through 30 MHz (R_L = 100Ω), 2.3 nV/$\overline{Hz}$ input referred noise, the LMH6738 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the LMH6738 low input referred noise and low harmonic distortion make it an attractive solution.

CONNECTION DIAGRAM

16-Pin SSOP
Top View



See Package Number DBQ0016A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V^+ - V^-)	13.2V
I_{OUT}	See Note (2)
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature Range	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

Operating Ratings (1)

Thermal Resistance		
Package	**(θ_{JC})**	**(θ_{JA})**
16-Pin SSOP	36°C/W	120°C/W
Operating Temperature Range	−40°C to +85°C	
Supply Voltage (V^+ - V^-)	8V to 12V	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.

Electrical Characteristics (1)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Performance						
UGBW	-3 dB Bandwidth	Unity Gain, V_{OUT} = 200 mV_{PP}		750		MHz
SSBW	-3 dB Bandwidth	V_{OUT} = 200 mV_{PP}		480		MHz
LSBW		V_{OUT} = 2 V_{PP}		400		
	0.1 dB Bandwidth	V_{OUT} = 2 V_{PP}		150		MHz
GFPL	Peaking	DC to 75 MHz		0		dB
GFR1	Rolloff	DC to 150 MHz, V_{OUT} = 2 V_{PP}		0.1		dB
GFR2	Rolloff	@ 300 MHz, V_{OUT} = 2 V_{PP}		1.0		dB
Time Domain Response						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.9		ns
TRL		5V Step		1.7		
SR	Slew Rate	5V Step		3300		V/µs
t_s	Settling Time to 0.1%	2V Step		10		ns
t_e	Enable Time	From $\overline{\text{Disable}}$ = rising edge.		7.3		ns
t_d	Disable Time	From $\overline{\text{Disable}}$ = falling edge.		4.5		ns
Distortion						
HD2L	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−80		dBc
HD2		2 V_{PP}, 20 MHz		−71		
HD2H		2 V_{PP}, 50 MHz		−55		
HD3L	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−90		dBc
HD3		2 V_{PP}, 20 MHz		−85		
HD3H		2 V_{PP}, 50 MHz		−65		
Equivalent Input Noise						
V_N	Non-Inverting Voltage	>1 MHz		2.3		nV/√Hz
I_{CN}	Inverting Current	>1 MHz		12		pA/√Hz
N_{CN}	Non-Inverting Current	>1 MHz		3		pA/√Hz
Video Performance						
DG	Differential Gain	4.43 MHz, R_L = 150Ω		.02		%
DP	Differential Phase	4.43 MHz, R_L = 150Ω		.01		°
Static, DC Performance						
VIO	Input Offset Voltage (2)			0.5	±2.5 **±4.5**	mV
IBN	Input Bias Current (2)	Non-Inverting	−15 **−20**	−7	0 **+5**	µA
IBI	Input Bias Current (2)	Inverting		−2	±25 **±35**	µA
PSRR	Power Supply Rejection Ratio (2)		50 **48.5**	53		dB
CMRR	Common Mode Rejection Ratio (2)		46 **44**	50		dB
XTLK	Crosstalk	Input Referred, f=10MHz, Drive channels A,C measure channel B		−80		dB
I_{CC}	Supply Current (2)	All three amps Enabled, No Load		32	35 **40**	mA
	Supply Current Disabled V^+	R_L = ∞		1.9	2.2	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

(2) Parameter 100% production tested at 25°C.

Electrical Characteristics [1] (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Supply Current Disabled V^-	R_L = ∞		1.1	1.3	mA
Miscellaneous Performance						
$R_{IN}+$	Non-Inverting Input Resistance			1000		kΩ
$C_{IN}+$	Non-Inverting Input Capacitance			.8		pF
$R_{IN}-$	Inverting Input Impedance	Output impedance of input buffer.		30		Ω
R_O	Output Impedance	DC		0.05		Ω
V_O	Output Voltage Range [2]	R_L = 100Ω	±3.25 **±3.1**	±3.5		V
		R_L = ∞	±3.65 **±3.5**	±3.8		
CMIR	Common Mode Input Range [2]	CMRR > 40 dB	±1.9 **±1.7**	±2.0		V
I_O	Linear Output Current [3] [2]	V_{IN} = 0V, V_{OUT} < ±30 mV	80 **60**	90		mA
I_{SC}	Short Circuit Current [4]	V_{IN} = 2V Output Shorted to Ground		160		mA
I_{IH}	Disable Pin Bias Current High	$\overline{\text{Disable}}$ Pin = V^+		10		µA
I_{IL}	Disable Pin Bias Current Low	$\overline{\text{Disable}}$ Pin = 0V		−350		µA
V_{DMAX}	Voltage for Disable	$\overline{\text{Disable}}$ Pin ≤ V_{DMAX}			0.8	V
V_{DMIM}	Voltage for Enable	$\overline{\text{Disable}}$ Pin ≥ V_{DMIN}	2.0			V

(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.

(4) Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Section for more details.

Typical Performance Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified).

Large Signal Frequency Response

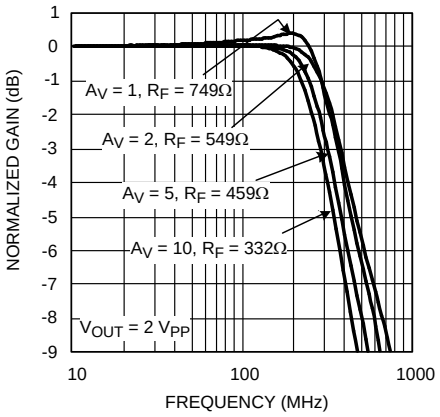


Figure 1.

Large Signal Frequency Response

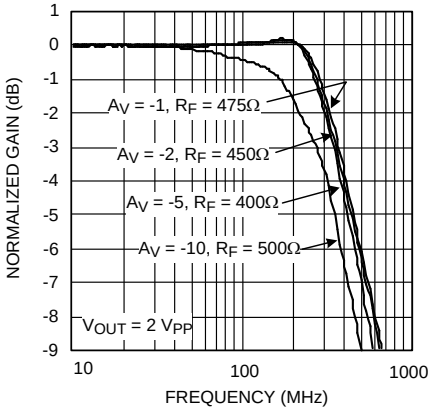


Figure 2.

Small Signal Frequency Response

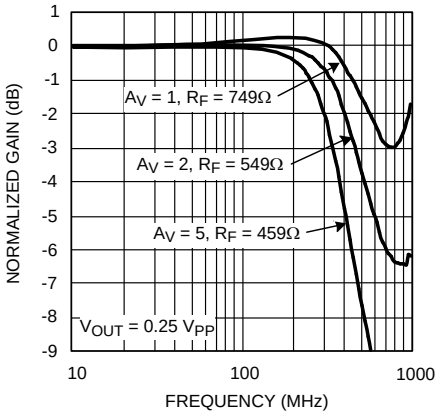


Figure 3.

Frequency Response vs. V_{OUT}

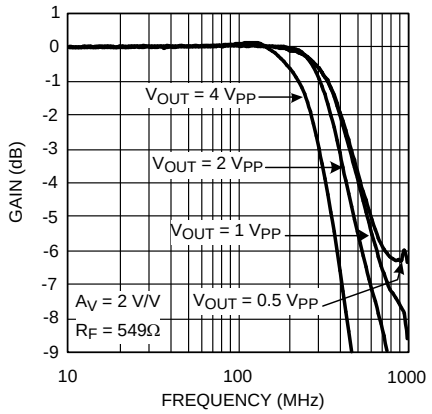


Figure 4.

Frequency Response vs. Supply Voltage

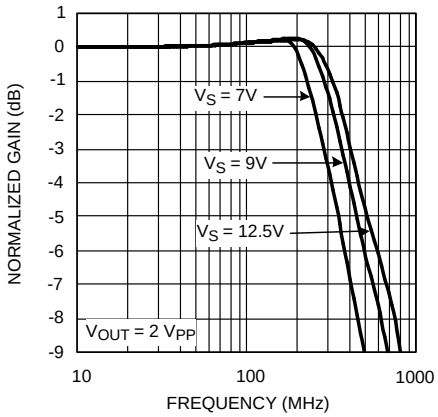


Figure 5.

Gain Flatness

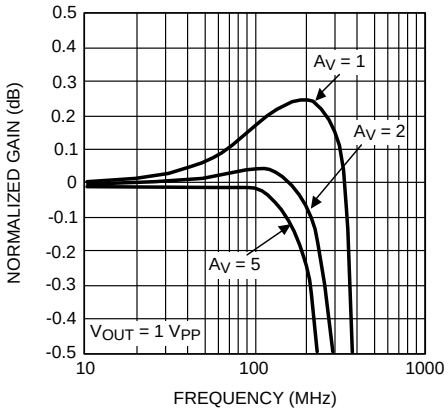


Figure 6.

Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified).

Pulse Response

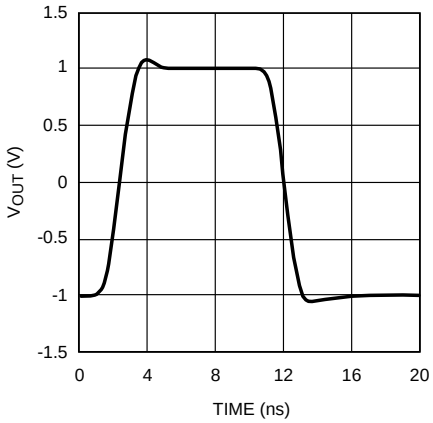


Figure 7.

Frequency Response vs. Capacitive Load

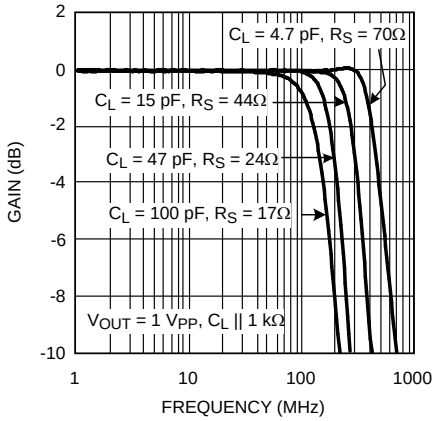


Figure 8.

Series Output Resistance vs. Capacitive Load

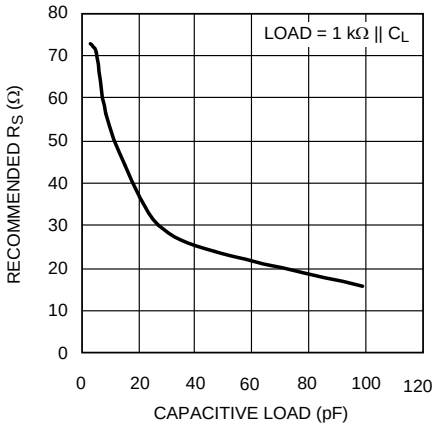


Figure 9.

Open Loop Gain and Phase

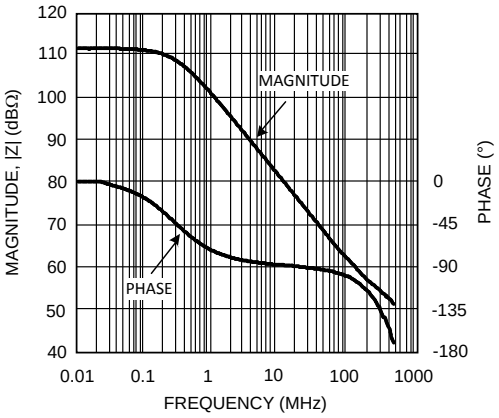


Figure 10.

Distortion vs. Frequency

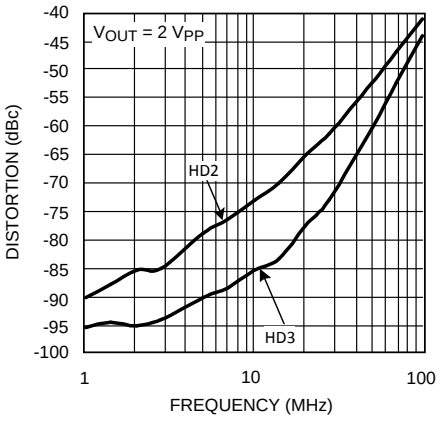


Figure 11.

Distortion vs. Output Voltage

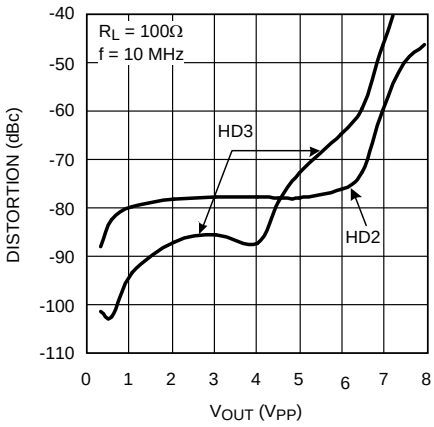


Figure 12.

Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified).

Distortion vs. Supply Voltage

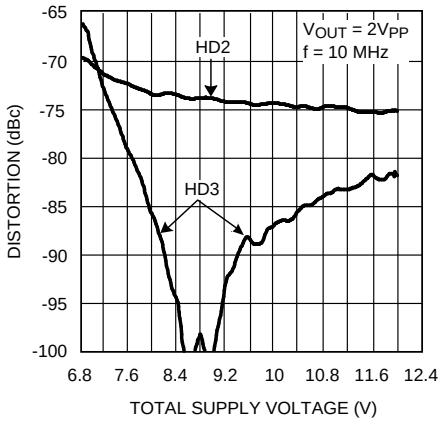


Figure 13.

CMRR vs. Frequency

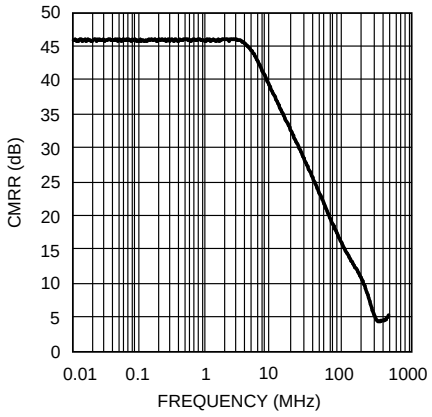


Figure 14.

PSRR vs. Frequency

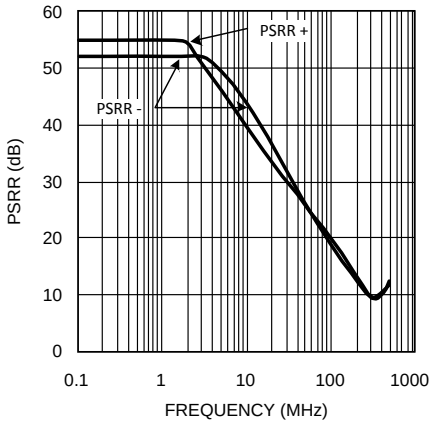


Figure 15.

Crosstalk vs. Frequency

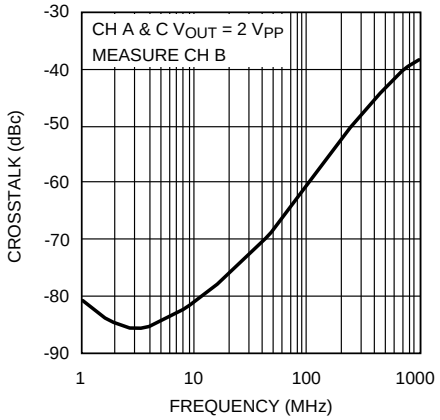


Figure 16.

Closed Loop Output Impedance |Z|

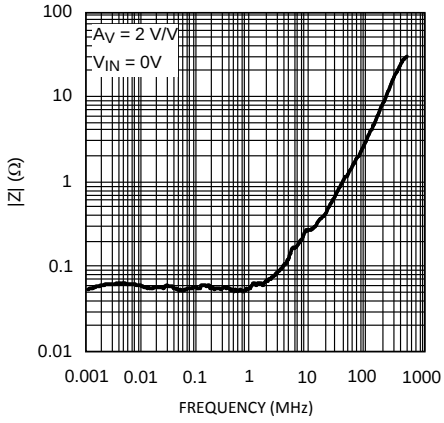


Figure 17.

Disable Timing

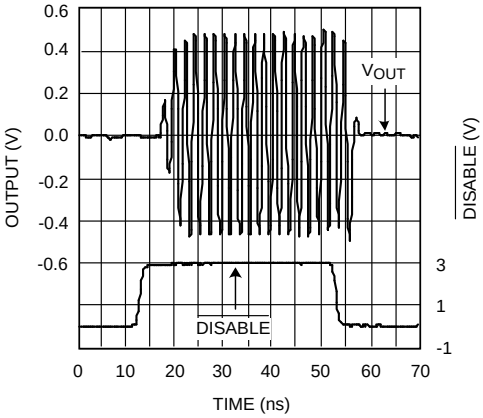


Figure 18.

Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_F = 549Ω; unless otherwise specified).

DC Errors vs. Temperature

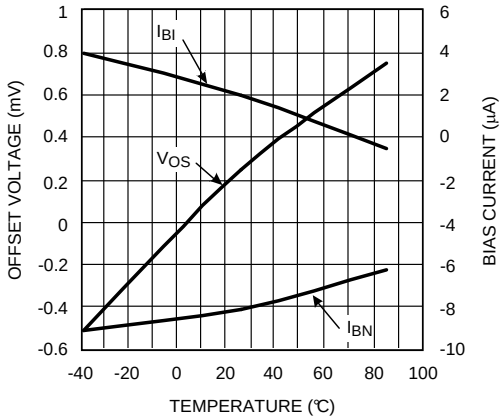


Figure 19.

Input Noise vs. Frequency

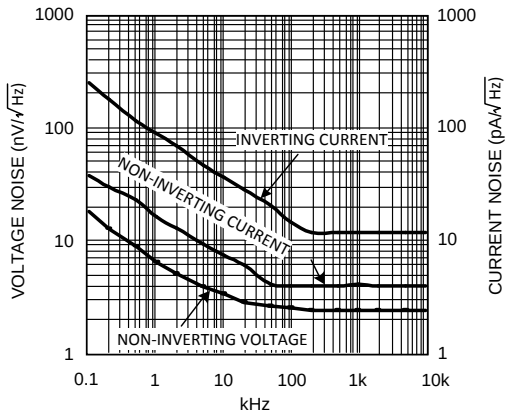
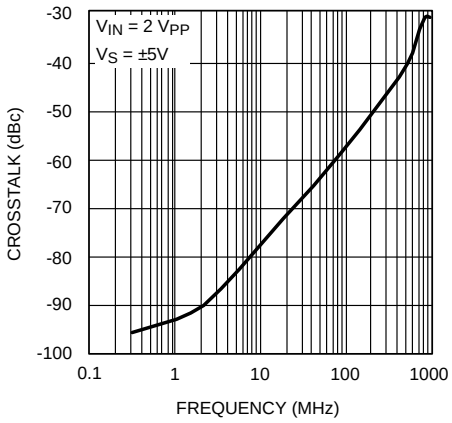


Figure 20.

Figure 21.

Disabled Channel Isolation vs. Frequency



APPLICATION INFORMATION

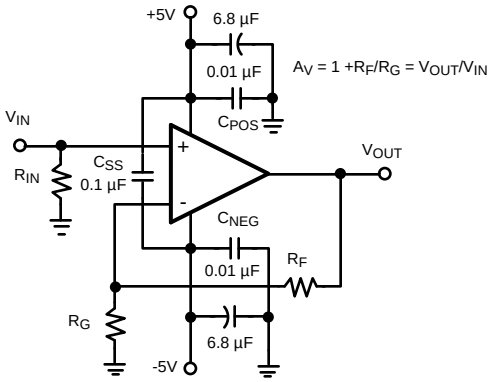


Figure 22. Recommended Non-Inverting Gain Circuit

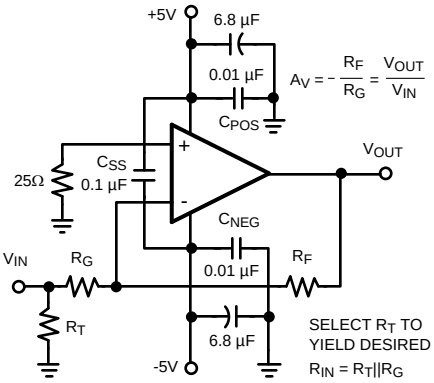


Figure 23. Recommended Inverting Gain Circuit

GENERAL INFORMATION

The LMH6738 is a high speed current feedback amplifier, optimized for very high speed and low distortion. The LMH6738 has no internal ground reference so single or split supply configurations are both equally useful.

EVALUATION BOARDS

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the data sheet plots were measured with these boards.

Device	Package	Evaluation Board Part Number
LMH6738MQA	SSOP	LMH730275

FEEDBACK RESISTOR SELECTION

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots specify an R_F of 550Ω, a gain of +2 V/V and ±5V power supplies (unless otherwise specified). Generally, lowering R_F from it's recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing and, eventually, oscillation.

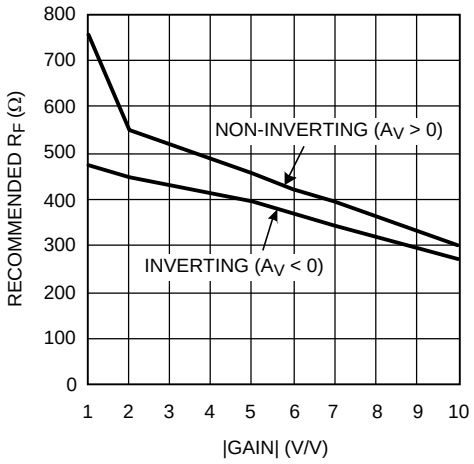


Figure 24. Recommended R_F vs. Gain

See Figure 24, Recommended R_F. vs Gain for selecting a feedback resistor value for gains of ±1 to ±10. Since each application is slightly different it is worth some experimentation to find the optimal R_F for a given circuit. In general a value of R_F that produces ~.1 dB of peaking is the best compromise between stability and maximal bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6738 requires a 750Ω feedback resistor for stable operation.

The LMH6738 was optimized for high speed operation. As shown in Figure 24 the suggested value for R_F decreases for higher gains. Due to the impedance of the input buffer there is a practical limit for how small $R_F$can go, based on the lowest practical value of R_G. This limitation applies to both inverting and non inverting configurations. For the LMH6738 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R_G. The LMH6738 begins to operate in a gain bandwidth limited fashion in the region where R_G is nearly equal to the input buffer impedance. Note that the amplifier will operate with R_G values well below 20Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the Inverting and Non Inverting inputs cannot be expected to remain small.

Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is R_G || R_T (R_T is optional). The value of R_G is R_F /Gain. Thus for an inverting gain of −7 V/V and an optimal value for R_F the input impedance is equal to 50Ω. Using a termination resistor this can be brought down to match a 25Ω source, however, a 150Ω source cannot be matched. To match a 150Ω source would require using a 1050Ω feedback resistor and would result in reduced bandwidth.

For more information see Application Note OA-13 (SNOA366) which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6738 is approximately 30Ω. The LMH6738 is designed for optimum performance at gains of +1 to +10 V/V and −1 to −9 V/V. Higher gain configurations are still useful, however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

ACTIVE FILTER

When using any current feedback Operational Amplifier as an active filter it is necessary to be careful using reactive components in the feedback loop. Reducing the feedback impedance, especially at higher frequencies, will almost certainly cause stability problems. Likewise capacitance on the inverting input should be avoided. See Application Notes OA-07 (SNOA365) and OA-26 (SNOA387) for more information on Active Filter applications for Current Feedback Op Amps.

When using the LMH6738 as a low pass filter the value of R_F can be substantially reduced from the value recommended in the R_F vs. Gain charts. The benefit of reducing R_F is increased gain at higher frequencies, which improves attenuation in the stop band. Stability problems are avoided because in the stop band additional device bandwidth is used to cancel the input signal rather than amplify it. The benefit of this change depends on the particulars of the circuit design. With a high pass filter configuration reducing R_F will likely result in device instability and is not recommended.

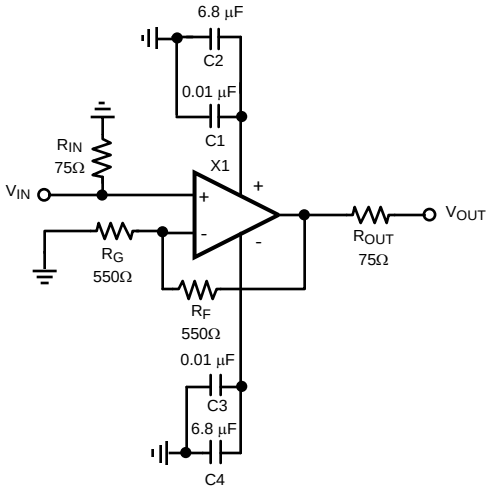


Figure 25. Typical Video Application

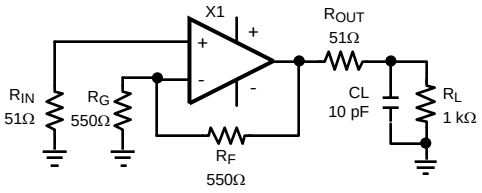


Figure 26. Decoupling Capacitive Loads

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 26 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The charts "Suggested R_{OUT} vs. Cap Load" give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

An alternative approach is to place Rout inside the feedback loop as shown in Figure 27. This will preserve gain accuracy, but will still limit maximum output voltage swing.

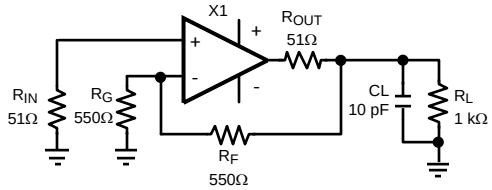


Figure 27. Series Output Resistor Inside Feedback Loop

INVERTING INPUT PARASITIC CAPACITANCE

Parasitic capacitance is any capacitance in a circuit that was not intentionally added. It comes about from electrical interaction between conductors. Parasitic capacitance can be reduced but never entirely eliminated. Most parasitic capacitances that cause problems are related to board layout or lack of termination on transmission lines. Please see the section on Layout Considerations for hints on reducing problems due to parasitic capacitances on board traces. Transmission lines should be terminated in their characteristic impedance at both ends.

High speed amplifiers are sensitive to capacitance between the inverting input and ground or power supplies. This shows up as gain peaking at high frequency. The capacitor raises device gain at high frequencies by making R_G appear smaller. Capacitive output loading will exaggerate this effect. In general, avoid introducing unnecessary parasitic capacitance at both the inverting input and the output.

One possible remedy for this effect is to slightly increase the value of the feedback (and gain set) resistor. This will tend to offset the high frequency gain peaking while leaving other parameters relatively unchanged. If the device has a capacitive load as well as inverting input capacitance using a series output resistor as described in DRIVING CAPACITIVE LOADS will help.

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board for the LMH6738.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6738 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In Figure 22 and Figure 23 C_{SS} is optional, but is recommended for best second harmonic distortion. Another option to using C_{SS} is to use pairs of .01 µF and 0.1 µF ceramic capacitors for each supply bypass.

VIDEO PERFORMANCE

The LMH6738 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 25 shows a typical configuration for driving a 75Ω Cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in R_{OUT}.

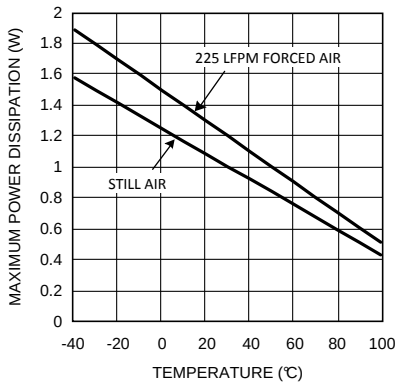


Figure 28. Maximum Power Dissipation

POWER DISSIPATION

The LMH6738 is optimized for maximum speed and performance in the small form factor of the standard SSOP-16 package. To achieve its high level of performance, the LMH6738 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used (V_S = ±5V, all 3 channels on). Therefore, it is easy to see the need for proper precautions to be taken in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation (all 3 channels).

With the LMH6738 used in a back-terminated 75Ω RGB analog video system (with 2 V_{PP} output voltage), the total power dissipation is around 435 mW of which 340 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, that puts the junction temperature to about 140° C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the SSOP-16 package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the SSOP-16 package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the Maximum power dissipation for the LMH6738:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}* (V_S)$ $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage:
   – P_D (rms) = rms $((V_S - V_{OUT})*I_{OUT})$ where V_{OUT} and I_{OUT} are the voltage and current across the external load and V_S is the total supply current
3. Calculate the total RMS power: $P_T = P_{AMP}+P_D$

The maximum power that the LMH6738, package can dissipate at a given temperature can be derived with the following equation (See Figure 28):

$P_{MAX} = (150^o - T_{AMB})/ \theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SSOP package θ_{JA} is 120°C/W.

ESD PROTECTION

The LMH6738 is protected against electrostatic discharge (ESD) on all pins. The LMH6738 will survive 2000V Human Body model and 200V Machine model events.

Under closed loop operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6738 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6738MQ/NOPB	ACTIVE	SSOP	DBQ	16	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 38MQ	Samples
LMH6738MQX/NOPB	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 38MQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

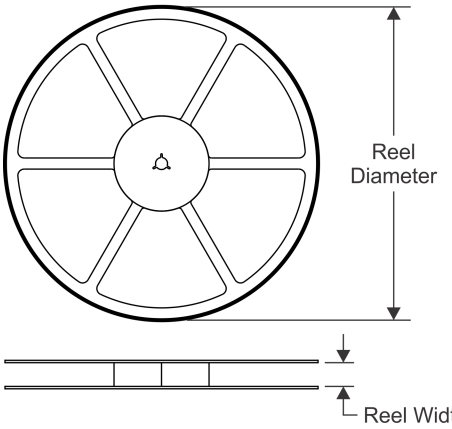
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

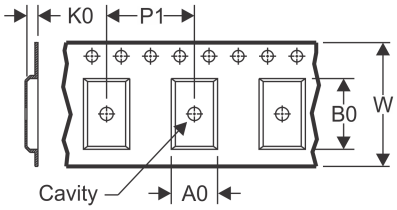
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

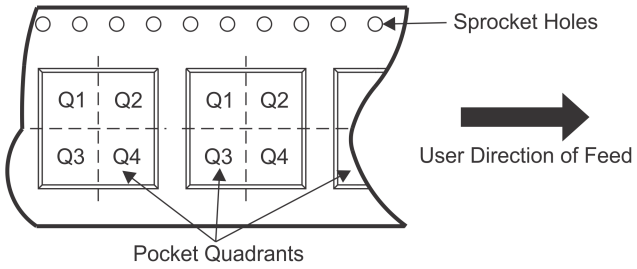


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

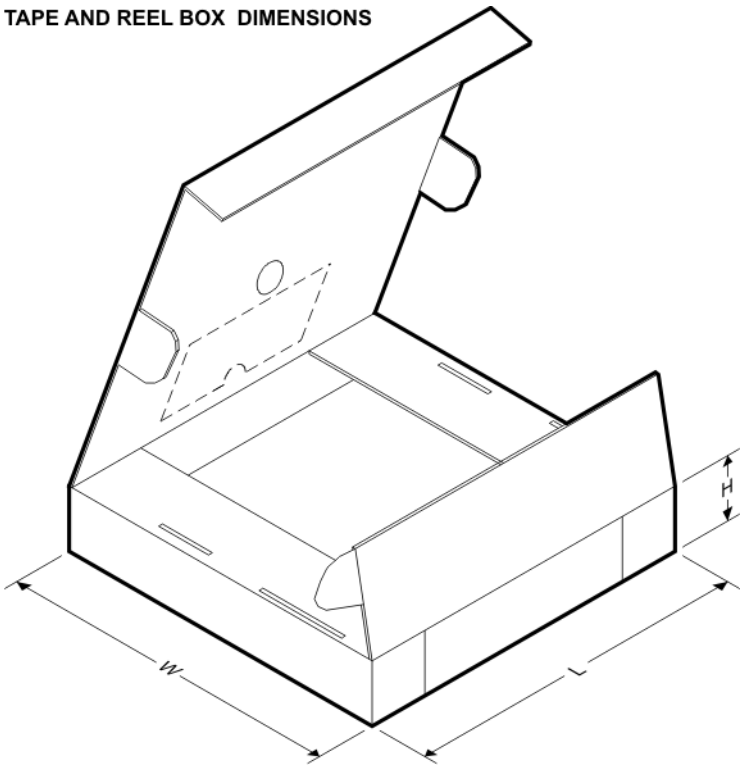
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6738MQX/NOPB	SSOP	DBQ	16	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

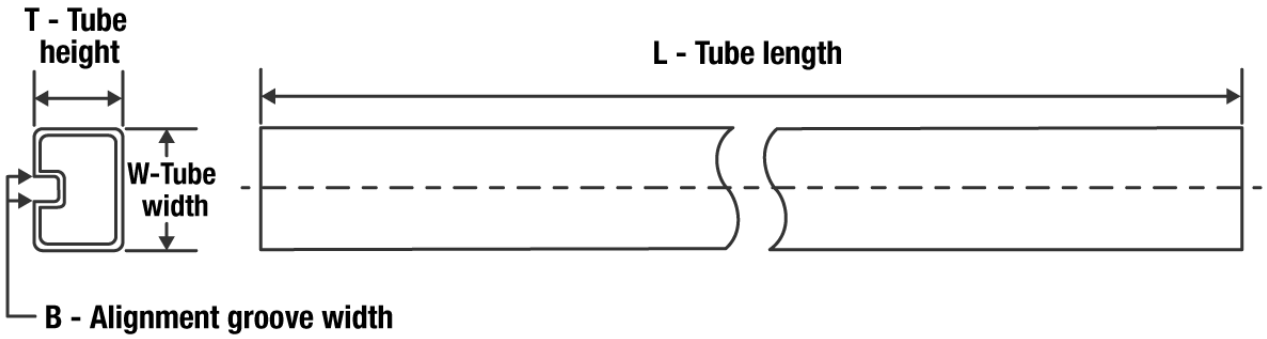
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

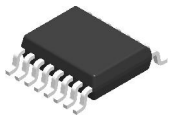
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6738MQX/NOPB	SSOP	DBQ	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6738MQ/NOPB	DBQ	SSOP	16	95	495	8	4064	3.05

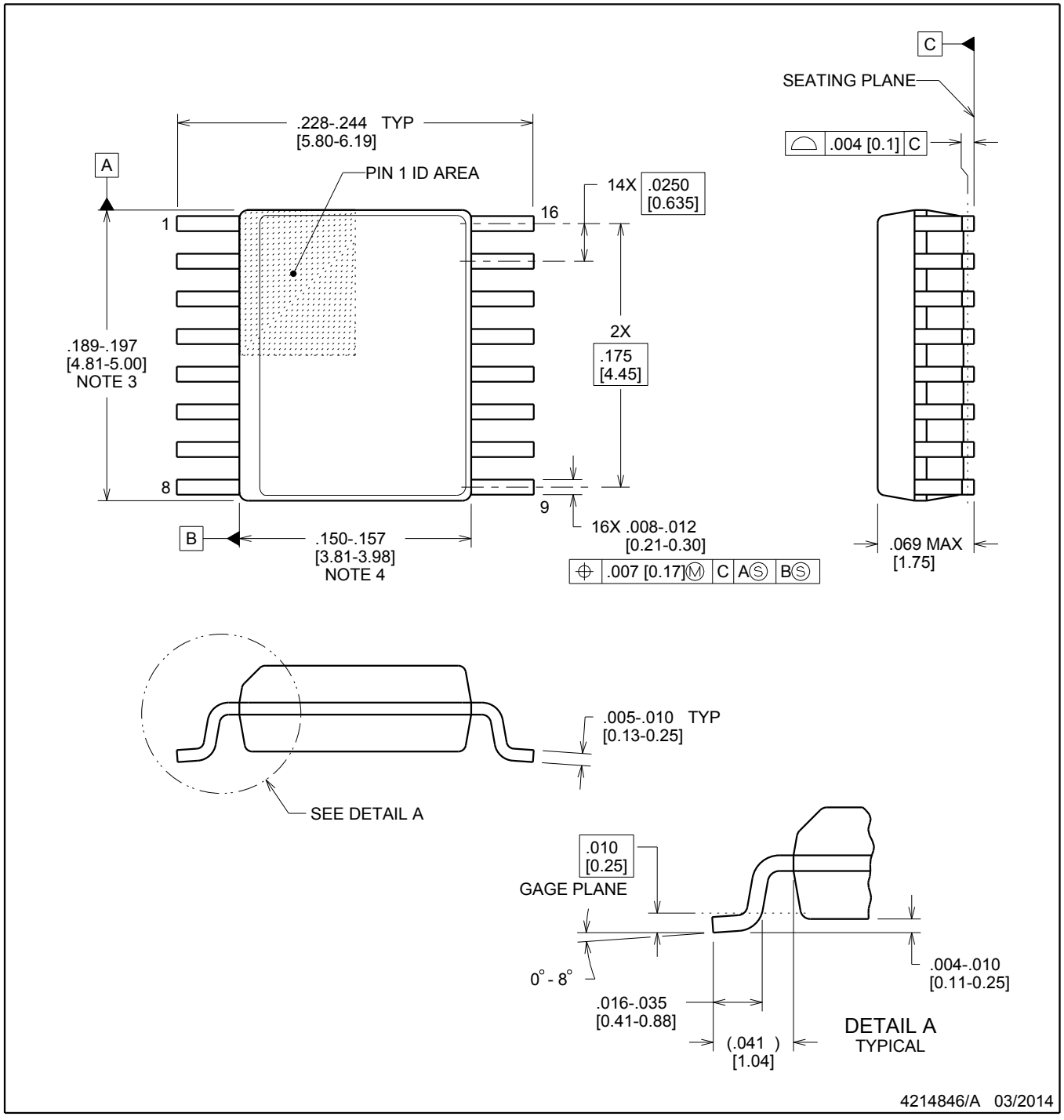


PACKAGE OUTLINE

DBQ0016A

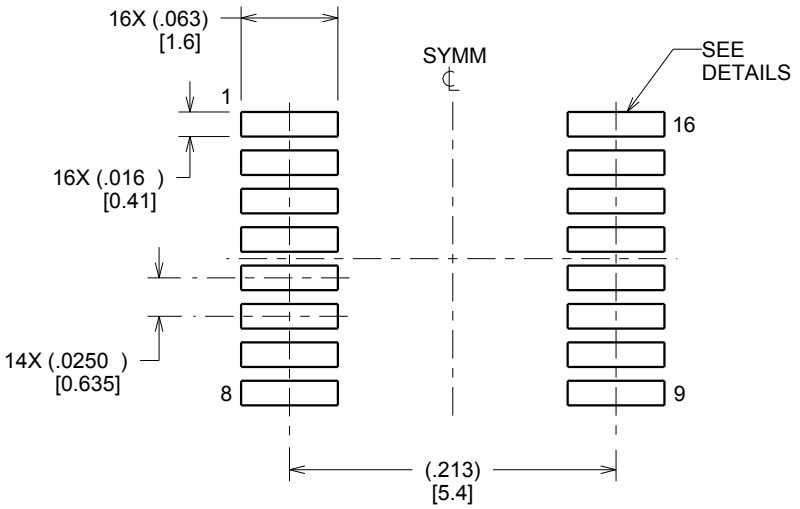
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

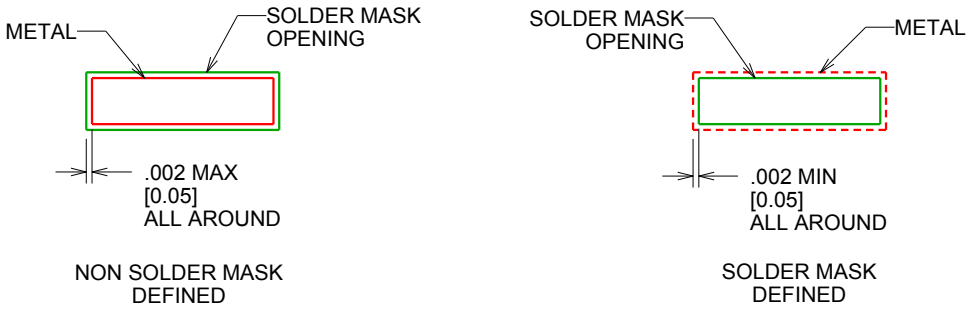


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

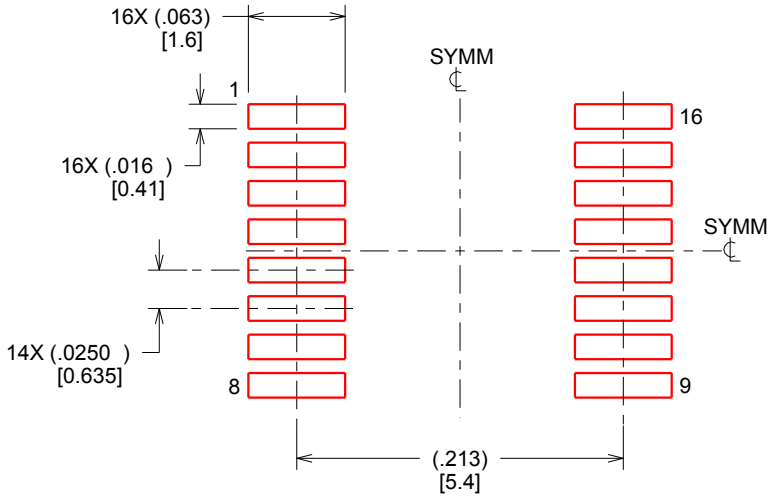
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265